F81768

LPC SIO with 2 UARTs

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Revision History

Revision Number	Revision Date	Description
0.10	April 2014	Initial release
0.11	May 2014	• Made correction and modification • Add section 4,5,6,7,8,9,10 and 11
0.12	July 2014	• Made correction and modification • In section 4.4.5, update function description of FAN_FAULT# • In section 4.5.3.5, update description of Keep last state new mode • In section 5.2.11, add register 28h [7] (FUNC_PROG_SEL = 1) • In section 5.2.13, correct description of 2Ah[7] • In section 5.2.13, correct description of 2Ah[4] • In section 5.2.14, correct description of 2Bh[4:0] • In section 5.10.5, correct description of F5h[1:0]

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1 General Description

The F81768 which is the featured IO chip for PC system is equipped with ATX/AT Strapping pin, which implements the Low Pin Count (LPC) interface, includes I/O functionally as well as motherboard glue logic into a 128-pin package.

The F81768 includes one IEEE 1284 Parallel Port, two UART Ports (COM Ports) with up to 128 bytes FIFO, provide 9 bit (multidrop) function, one 80 port (multi with COM2), Hardware Keyboard Controller (KBC), and SIR. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.The F81768 integrates with hardware monitor, 11 sets of voltage sensor, 3 sets of creative auto-controlling fans and 3 temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external transistors 2N3906. Others, the F81768 supports newest AMD TSI, Intel PECI 3.0 interfaces, MXM and SMBus (master & slave) for temperature sensing and provides the power sequence controller function for AMD platform.

The F81768 provides flexible features for multi-directional application. For instance, the F81768 provides 61 GPIO pins (multi-pin), IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Manual Mode/Stage Auto Mode/Linear Auto Mode for users' selection.

In order to save the current consumption when the system is in the soft off state which is so called power saving function. The power saving function supports that system boot-on not only by pressing the power button but also by the wake-up events via GPIO3x, GPIO5x & RI#. When the system enters the S4/S5 state, F81768 can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be simulated to G3-like state when system enters the S4/S5 states. At the G3-like state, the F81768 consumes the 5VA power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfill a low power consumption system which supports a wake up function.

These features as above description will help you more and improve the product value. The F81768 is powered by 3.3V voltage, with the LPC interface in the green package of 128-LQFP (14mm*14mm).

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2 Feature Overview

General Functions

- Comply with LPC Spec. 1.1
- Support DPM (Device Power Management), ACPI
- Support AMD power sequence controller
- Provides two UARTs with programmable 16/32/64/128 bytes FIFO
  - Multi drop function
  - Support IRQ Sharing function.
  - Provide auto flow control function
- Hardware KBC and Parallel Port
- H/W monitor functions
- Support AMD TSI, MXM, Intel PECI 3.0 interface
- Provide SMBus slave & master function
- Provide 3 sets of SMBus Interface.
- 61 GPIO Pins for flexible application
- Provide Power Saving Function (Comply ERP lot 6.0)
- Support Intel Deep Sleep Well (DSW) Timing Sequence
- Provide ATX emulates AT Function
- 24/48 MHz clock input
- Packaged in 128-LQFP and powered by 3.3VCC

Intel Platform

- Support Intel® Deep Sleep Well (DSW)
- Support Intel® PECI 3.0

AMD Platform

- Support AMD® Power Sequence (Group A and Group B)

UART

- Two high-speed 16C550/16C650/16C750/16C850/16C950 compatible UART with programmable 16/32/64/128 bytes FIFO
- Baud rate up to 115.2K, max. up to 1.5M
- Support IRQ sharing
- Support Ring-In Wakeup
- Provide auto flow control function
- Provide Multi drop (9-bits) Function for Gaming Machine
- Support programmable register for TX/RX only, Modem control, & fully UART function

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

80-Port Interface

- Monitor 0x80 Port and output the value via signals defined for 7-segment display.
- High nibble and low nibble are outputted interleaved at 1KHz frequency.
- 80-Port output via COM2 interface.
- Provide MXM/PECI/TSI/T1/T2/T3 value via 80-port

Parallel Port

- One PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Hardware Monitor Functions

- 3 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- Temperature range -40℃~127℃
- 11 sets voltage monitoring (6 external and 5 internal powers)
- Voltage monitor supports Over Voltage Protection (OVP)

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- High limit signal (PME#) for Vcore level
- 3 fan speed monitoring inputs
- 3 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- The Fan PWM output frequency can be programmed as 23.5/11.75/5.875KHz, & 200Hz for LCD backlight adjustment
- Stage auto mode (2-Limit and 3-Stage)/Linear auto mode/Manual mode
- OVT# hardware signals output
- Case open detection (assert via PME/BEEP)
- WATCHDOG comparison of all monitored values
- PSIN# detection time flag is programmable 1s(default)/2s/3s/4s (Enter BIOS setting page under the quick booting WIN8/WIN8.1 OS)

Keyboard Controller
- LPC interface support serial interrupt channel 1, 12.
- Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
- Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.
- Programmable compatibility with the 8042.
- Support both interrupt and polling modes.
- Fast Gate A20 and Hardware Keyboard Reset.

ACPI
- Provide ATX Emulates AT Function

Power Saving Controller
- ACPI Timing and Power Control
- Wake-up Supported
- G3-like Timing Control
- Comply With ERP Lot 6.0
- Built in Soft Start Function for Two Control Pins with VSB Power Sources Control.
- Event in input via EVENT_IN, GPIO0x (except GPIO07), GPIO1x , GPIO3x, GPIO44~47, GPIO 5x, RI# pins

GPIO Function
- Total 61 pins GPIO
- GPIO0x , GPIO1x , GPIO3x, GPIO4x, GPIO5x, GPIO6x support SMI wake up via PME# or SIRQ
- GPIO0x, GPIO3x, GPIO5x could be reset by 3VA/VBAT via the register setting
- Scan Code
  - Support Scan Code Via GPIO6x
  - GPIO64~67 support programmable combination keys (single or dual code: Clt + Alt + code)
- All GPIO supports digit IO for Input/Output control, Output data control, input status.
- Support High/Low Level/Pulse, Open Drain/Push Pull function selection

Watch Dog Timer
- Time resolution minute/second
- Maximum 256 minutes or 256 seconds
- Output signal via WDTRST#/PWROK/PCI_RST4#
- WDT could also wake up via PME#, PSOUT#
- Provide hardware strapping pin & auto reload function

AMD TSI/MXM/I^{2}C Interface
- Support slave interface to report the hardware monitor data under S0/S3/S5
- I2C slave default address is 5Ch
- Support master interface to get the thermal data via PCH & MXM module
- Provide 3 sets of SMBus for TSI/MXM/I^{2}C interface.
- AMD TSI/MXM/I2C interfaces could be selected individually via 4 sets of pins
  - pin 49 (GPIO00/TSI_SCL/I^{2}C_SCL), & pin 50 (GPIO01/TSI_SDA/I^{2}C_SDA);
  - pin 51 (GPIO02/TSI_SCL/I^{2}C_SCL), & pin 52 (GPIO03/TSI_SDA/I^{2}C_SDA);
  - pin 57 (GPIO06/TSI_SCL/I^{2}C_SCL), & pin 58 (PECI/TSI_SDA/I^{2}C_SDA);
  - pin 71 (MDATA/TSI_SDA/I^{2}C_SDA), & pin 72(MCLK/TSI_SCL/I^{2}C_SCL).

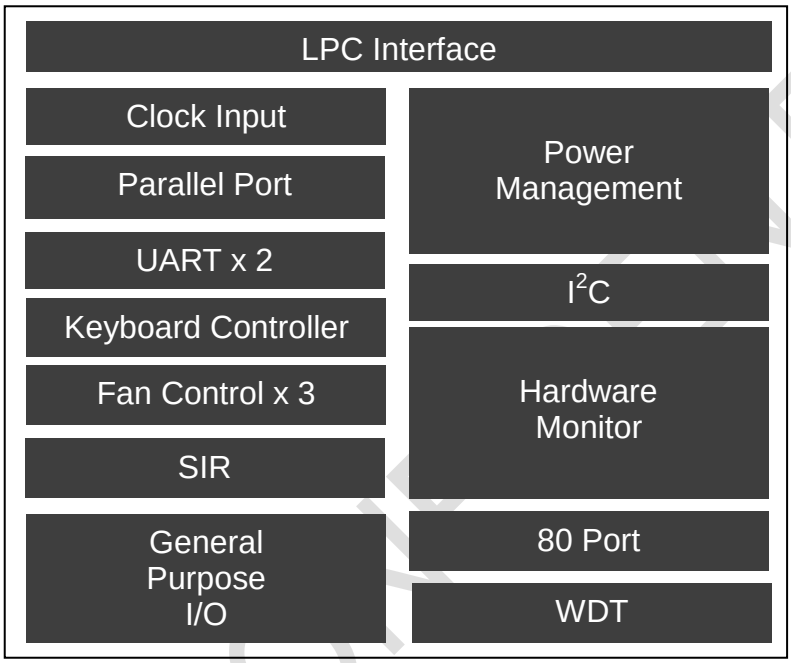
Package
- 128-pin LQFP (14mm*14mm) Green Package

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3 Signal/Pin Connection and Description

3.1 Block Diagram

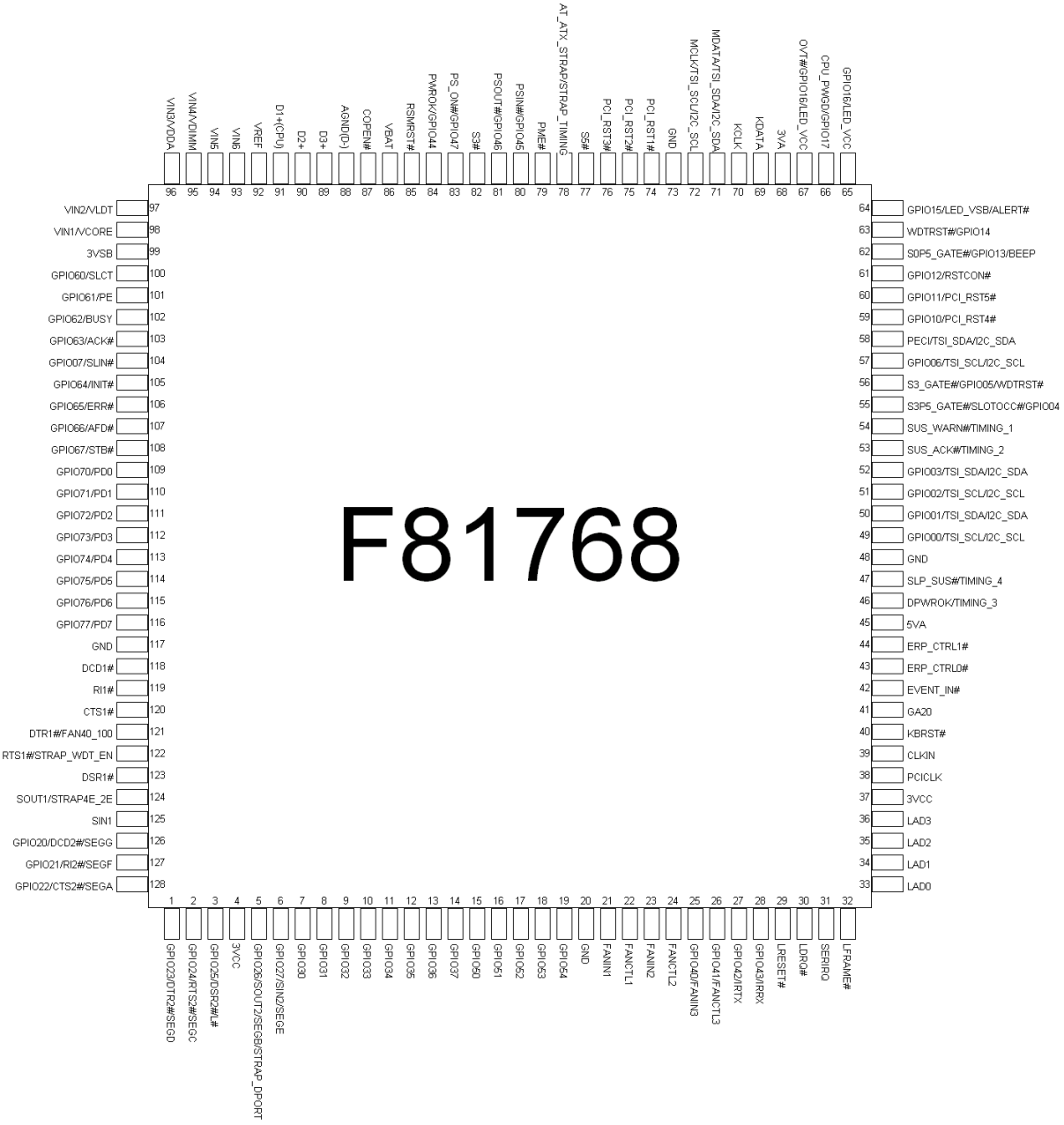
Figure 1 Block diagram



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3.2 Pin Connection Configuration

Figure 2 Pin Configuration



3.3 Pin Description

3.3.1 Power Pins

Table 1 Power pins description

No	Name	Type	Description
4,37	3VCC	P	Power supply voltage input with 3.3V. This pin support OVP/UVP function, and default is disabled.
45	5VA	P	5V standby power input (via ATX Power). Provide 5VA voltage detection & power good signal for DPWROK function.
68	3VA	P	3.3V stand by power input (via ATX Power). Power detection for the rising is 2.8V & falling is 2.5V. Provide 3VA voltage detection & power good signal for DPWROK function.
86	VBAT	P	Battery voltage input where power good level is 2.0V. Provide VBAT detection function.
88	AGND(D-)	P	Analog GND
99	3VSB	P	Analog Stand-by power supply voltage input 3.3V.
20, 48, 73, 117	GND	P	Digital GND

3.3.2 LPC Interface

Table 2 LPC pins description

No	Name	Type	PWR	Description
29	LRESET#	$IN_{st,5v}$	3VCC	Reset signal. It can connect to PCI_RST# signal on the host.
30	LDRQ#	O_{16}	3VCC	Encoded DMA Request signal.
31	SERIRQ	$I/O_{16t,u47k}$	3VCC	Serial IRQ input/output.
32	LFRAME#	$IN_{st,u47k}$	3VCC	Indicates start of a new cycle or termination of a broken cycle.
33-36	LAD[0:3]	$I/O_{16t,u47k}$	3VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
38	PCICLK	$IN_{st,5v}$	3VCC	25/33MHz PCI clock input.

3.3.3 Clock

Table 3 Clock pin description

No	Name	Type	PWR	Description
39	CLKIN	$IN_{st,5v}$	3VCC	System clock input. According to the input frequency 24/48MHz.

3.3.4 Serial Infrared (SIR)

Table 4 SIR pins description

No	Name	Type	PWR	Description

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27	GPIO42	$I/OOD_{12t,5v}$	3VCC	Default General Purpose IO.
	IRTX	O_{12}		Infrared Transmitter Output. The function is selected by register setting.
28	GPIO43	$I/OOD_{12t,5v}$	3VCC	Default General Purpose IO.
	IRRX	$IN_{st,5v}$		Infrared Receiver input. The function is selected by register setting.

3.3.5 Serial I/O Universal Asynchronous Receiver Transmitter (UART), 80 Port Interface

Table 5 UART and 80 Port pins description

No	Name	Type	PWR	Description
118	DCD1#	$IN_{st,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
119	RI1#	$IN_{st,5v}$	3VA	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
120	CTS1#	$IN_{st,5v}$	3VCC	Clear To Send is the modem control input.
121	DTR1#	$O_{8t,5v,u47k}$	3VCC	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	FAN40_100	IN_{t5v}		Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 40%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
122	RTS1#	$O_{8t,5v,u47k}$	3VCC	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
	STRAP_WDT_EN	IN_{t5v}		Power on strapping: (Internal pull high) 1 (Default):Disable WDT 0 :Enable WDT
123	DSR1#	$IN_{st,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
124	SOUT1	$O_{8t,5v,u47k}$	3VCC	UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	STRAP4E_2E	IN_{t5v}		Power on strapping: 1(Default): Configuration register 4E 0: Configuration register 2E
125	SIN1	$IN_{st,5v}$	3VCC	Serial Input. Used to receive serial data through the communication link.
126	GPIO20	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.

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	DCD2#	$IN_{st,5v}$		Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier. The function is selected by register setting.
	SEGG	O_{18}		SEGG for 7-segment display. (Select by pin 5 power on strapping)
127	GPIO21	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	RI2#	$IN_{st,5v}$		Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set. The function is selected by register setting.
	SEGF	O_{18}		SEGF for 7-segment display. (Select by pin 5 power on strapping)
128	GPIO22	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	CTS2#	$IN_{st,5v}$		Clear To Send is the modem control input. The function is selected by register setting.
	SEGA	O_{18}		SEGA for 7-segment display. (Select by pin 5 power on strapping)
1	GPIO23	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	DTR2#	$O_{8t,5v,u47k}$		UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. The function is selected by register setting.
	SEGD	O_{18}		SEGD for 7-segment display. (Select by pin 5 power on strapping)
2	GPIO24	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	RTS2#	$O_{8t,5v,u47k}$		UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. The function is selected by register setting.
	SEGC	O_{18}		SEGC for 7-segment display. (Select by pin 5 power on strapping)
3	GPIO25	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	DSR2#	$IN_{st,5v}$		Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART. The function is selected by register setting.
	L#	O_{30}		L# for 7-segment display. (Select by pin 5 power on strapping)
5	GPIO26	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	SOUT2	$O_{8t,5v,u47k}$		UART 2 Serial Output. Used to transmit serial data out to the communication link. The function is selected by register setting.
	SEGB	O_{18}		SEGB for 7-segment display. (Select by pin 5 power on strapping)
	STRAP_DPORT	IN_{t5v}		Strap for 80 Port. Default internal Pull High for 80 Port Enable.
6	GPIO27	$I/OOD_{8st,5v}$	3VCC	Default General Purpose IO.
	SIN2	$IN_{st,5v}$		Serial Input. Used to receive serial data through the communication link. The function is selected by register setting.
	SEGE	O_{18}		SEGE for 7-segment display. (Select by pin 5 power on strapping)

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3.3.6 Parallel Port (LPT Port)

Table 6 LPT pins description

No	Name	Type	PWR	Description
100	GPIO60	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	SLCT	$IN_{st,5v}$		An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
101	GPIO61	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PE	$IN_{st,5v}$		An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
102	GPIO62	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	BUSY	$IN_{st,5v}$		An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
103	GPIO63	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	ACK#	$IN_{st,5v}$		An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
104	GPIO07	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	SLIN#	$I/OOD_{12st,5v}$		Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
105	GPIO64	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	INIT#	$I/OOD_{12st,5v}$		Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
106	GPIO65	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	ERR#	$IN_{st,5v}$		An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
107	GPIO66	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	AFD#	$I/OOD_{12st,5v}$		An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
108	GPIO67	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	STB#	$I/OOD_{12st,5v}$		An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
109	GPIO70	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD0	$I/O_{12st,5v}$		Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

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110	GPIO71	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD1	$I/O_{12st,5v}$		Parallel port data bus bit 1.
111	GPIO72	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD2	$I/O_{12st,5v}$		Parallel port data bus bit 2.
112	GPIO73	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD3	$I/O_{12st,5v}$		Parallel port data bus bit 3.
113	GPIO74	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD4	$I/O_{12st,5v}$		Parallel port data bus bit 4.
114	GPIO75	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD5	$I/O_{12st,5v}$		Parallel port data bus bit 5.
115	GPIO76	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD6	$I/O_{12st,5v}$		Parallel port data bus bit 6.
116	GPIO77	$I/OOD_{12t,5v}$	3VCC	General Purpose IO.
	PD7	$I/O_{12st,5v}$		Parallel port data bus bit 7.

3.3.7 Hardware Monitor

Table 7 Hardware monitor pins description

No	Name	Type	PWR	Description
93	VIN6	AIN	3VSB	Voltage input 6. This pin support OVP/UVP function, and default is disabled.
94	VIN5	AIN	3VSB	Voltage input 5. This pin support OVP/UVP function, and default is disabled.
95	VIN4/VDIMM	AIN	3VSB	Voltage input 4 or VDIMM input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
96	VIN3/VDDA	AIN	3VSB	Voltage input 3 or VDDA input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
97	VIN2/VLDT	AIN	3VSB	Voltage input 2 or VLDT input used in AMD platform. The input voltage level for timing control usage must be over 1V after voltage divider.
98	VIN1/VCORE	AIN	3VSB	Voltage Input for VCORE. The input voltage level for timing control usage must be over 0.7V.
21	FANIN1	$IN_{st,5v}$	3VCC	Fan 1 tachometer input.

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22	FANCTL1	$OOD_{12,5v}$ AOUT	3VCC	Fan 1 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down 100k internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
23	FANIN2	$IN_{st,5v}$	3VCC	Fan 2 tachometer input.
24	FANCTL2	$OOD_{12,5v}$ AOUT	3VCC	Fan 2 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down 100k internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
25	GPIO40	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
	FANIN3	$IN_{st,5v}$		Fan 3 speed input. This function is selected by register setting.
26	GPIO41	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
	FANCTL3	$OOD_{12,5v}$ AOUT		Fan 3 control output. It is also a trap pin to select a PWM or a DAC output, except being an output pin. It defaults to be a voltage output by pulling down 100k internally. It is set as a PWM output as connected a 4.7K resistor and pulled high to 3.3V. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
57	GPIO06	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	TSI_SCL	$OD_{12st,5v}$		Clock output for AMD TSI.
	I2C_SCL	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface CLOCK pin.
58	PECI	$I_{Lv}/O_{D8,S1}$	3VSB	Intel PECI hardware monitor interface. When TIMING_GPIO pin is set in GPIO function (INTEL mode). PECI function can be set by the register.
	TSI_SDA	$I_{Lv}/OD_{12st,5v}$		AMD TSI Interface DATA pin.
	I2C_SDA	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface DATA pin.
63	WDTRST#	$OD_{12,5v}$	3VSB	Watch dog timer signal output.
	GPIO14	$I/OOD_{12st,5v}$		General Purpose IO. GPIO function is selected by register setting
67	OVT#	$OD_{12,5v}$	3VSB	Over temperature signal output.
	GPIO16	$I/OOD_{12st,5v}$		General Purpose IO.
	LED_VCC	$OD_{12,5v}$		Power LED for VCC. This function is selected by the register setting.
79	PME#	$OD_{12,5v}$	3VSB	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.
89	D3+	AIN	3VSB	Thermal diode/transistor temperature sensor input for system use.
90	D2+	AIN	3VSB	Thermal diode/transistor temperature sensor input.

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91	D1+(CPU)	AIN	3VSB	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	VREF	AOUT	3VSB	Voltage sensor output.

3.3.8 Keyboard and Mouse Controller (KBC)

Table 8 KBC pins description

No	Name	Type	PWR	Description
40	KBRST#	$OD_{16,5v,u10k}$	3VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
41	GA20	$OD_{16,5v,u10k}$	3VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
69	KDATA	$I/OD_{16st,5V}$	3VSB	Keyboard Data.
70	KCLK	$I/OD_{16st,5V}$	3VSB	Keyboard Clock.
71	MDATA	$I/OD_{16st,5V}$	3VSB	PS2 Mouse Data.
	TSI_SDA	$I_{Lv}/OD_{12st,5v}$		AMD TSI Interface DATA pin.
	I2C_SDA	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface DATA pin.
72	MCLK	$I/OD_{16st,5V}$	3VSB	PS2 Mouse Clock.
	TSI_SCL	$OD_{12st,5v}$		Clock output for AMD TSI.
	I2C_SCL	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface CLOCK pin.

3.3.9 General-Purpose I/O (GPIO)

Table 9 GPIO pins description

No	Name	Type	PWR	Description
7	GPIO30	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
8	GPIO31	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
9	GPIO32	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
10	GPIO33	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
11	GPIO34	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
12	GPIO35	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
13	GPIO36	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
14	GPIO37	$I/OD_{14st,5v}$	3VCC	General Purpose IO.
15	GPIO50	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
16	GPIO51	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
17	GPIO52	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
18	GPIO53	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
19	GPIO54	$I/OOD_{12st,5v}$	3VCC	General Purpose IO.
49	GPIO00	I/OOD_{12t}	3VSB	General Purpose IO.

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	TSI_SCL	$OD_{12st,5v}$		Clock output for AMD TSI.
	I2C_SCL	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface CLOCK pin.
50	GPIO01	I/OOD_{12t}	3VSB	General Purpose IO.
	TSI_SDA	$I_{Lv}/OD_{12st,5v}$		AMD TSI Interface DATA pin.
	I2C_SDA	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface DATA pin.
51	GPIO02	I/OOD_{12t}	3VSB	General Purpose IO.
	TSI_SCL	$OD_{12st,5v}$		Clock output for AMD TSI.
	I2C_SCL	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface CLOCK pin.
52	GPIO03	I/OOD_{12t}	3VSB	General Purpose IO.
	TSI_SDA	$I_{Lv}/OD_{12st,5v}$		AMD TSI Interface DATA pin.
	I2C_SDA	$I_{Lv}/OD_{12st,5v}$		SMBUS Interface DATA pin.

3.3.10 ACPI

Table 10 ACPI pins description

No	Name	Type	PWR	Description
59	GPIO10	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	PCI_RST4#	$O_{12,5v}$		It is an output buffer of LRESET#. WDT function could be asserted via this pin
60	GPIO11	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	PCI_RST5#	$O_{12,5v}$		It is an output buffer of LRESET#
61	GPIO12	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	RSTCON#	$IN_{st,5v}$		Reset button input. This signal could be asserted via PWROK/PCI_RST4#/PCI_RST5#.
64	GPIO15	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	LED_VSB	$OD_{12,5v}$		Power LED for VSB.
	ALERT#	$OD_{12,5v}$		Alert a signal when temperature over limit setting.
65	GPIO16	$I/OOD_{12st,5v}$	3VSB	General Purpose IO.
	LED_VCC	$OD_{12,5v}$		Power LED for VCC.
66	CPU_PWGD	$OD_{12,5v}$	3VSB	CPU Power Good signal output (Detected by VIN1~VIN4 level good).
	GPIO17	$I/OOD_{12st,5v}$		General Purpose IO.
74	PCI_RST1#	$OD_{12,5v}$	3VSB	It is an output buffer of LRESET#.
75	PCI_RST2#	$O_{12,5v}$	3VSB	It is an output buffer of LRESET#.
76	PCI_RST3#	$O_{12,5v}$	3VSB	It is an output buffer of LRESET#.
77	S5#	$IN_{st,5v}$	3VSB	S5# signal input.
78	AT_ATX_ST	INt,5v	3VSB	Power on trapping: ATX emulates AT function

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	RAP			1: ATX mode (Default, internal pull high 47k Ω). 0: AT mode. The external resisters are necessary to decide the mode. Check the power on strapping section for the detail.
	STRAP_TIMING	$IN_{st,5v}$		Strap Pin for AMD and Intel timing. Internal pull high with AMD timing (Default). The external resisters are necessary to decide the mode. Check the power on strapping section for the detail.
80	PSIN#	$IN_{st,5v}$	3VSB	Main power switch button input.
	GPIO45	$I/OOD_{12st,5v}$		General Purpose IO.
81	PSOUT#	$OD_{12,5v}$	3VSB	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO46	$I/OOD_{12st,5v}$		General Purpose IO.
82	S3#	$IN_{st,5v}$	3VSB	S3# Input is Main power on-off switch input.
83	PS_ON#	$OD_{12,5v}$	3VSB	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
	GPIO47	$I/OOD_{12st,5v}$		General Purpose IO.
84	PWROK	$OD_{12,5v}$	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V. The additional PWROK delay is programmable 100ms/200ms (Default)/400ms.
	GPIO44	$I/OOD_{12st,5v}$		General Purpose IO.
85	RSMRST#	$OD_{12,5v,u10k}$	VBAT	Resume Reset# function, It is power good signal of VSB, which rises delayed 66ms as VSB arrives at 2.8V and falls as VSB drops to 2.6V. There is an option to set RSMRST# rises at 3.05V and falls at 2.95V.
87	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop backed by the battery for case open state preservation during power loss.

3.3.11 Power Saving

Table 11 Power saving pins description

No	Name	Type	PWR	Description
42	EVENT_IN#	$IN_{st,5v}$	3VSB	Wake-up event input. The signal input wakes the system up from the sleep state.
43	ERP_CTRL0#	OD_{12}	3VSB	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
44	ERP_CTRL1#	OD_{12}	3VSB	Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
46	DPWROK	$OD_{12,5v}$	3VSB	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.

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<table>
<tr><td></td><td>TIMING_3</td><td>$OD_{12,5v}$</td><td></td><td>Active high. Timing sequence 3 of power on/off sequence pins. The external pull high resistor is required.
(Detected by VIN3 level good)</td></tr>
<tr><td rowspan="2">47</td><td>SLP_SUS#</td><td>$IN_{st,lv}$</td><td rowspan="2">3VSB</td><td>For Intel CPT DSW function. Connect to PCH SLP_SUS pin.</td></tr>
<tr><td>TIMING_4</td><td>$OD_{12,5v}$</td><td>Active high. Timing sequence 4 of power on/off sequence pins. The external pull high resistor is required.
(Detected by VIN1 level good)</td></tr>
<tr><td rowspan="2">53</td><td>SUS_ACK#</td><td>$OOD_{16,5v}$</td><td rowspan="2">3VSB</td><td>This pin must wait SUS_WARN# signal for entering DSW power state.</td></tr>
<tr><td>TIMING_2</td><td>$OD_{12,5v}$</td><td>Active high. Timing sequence 2 of power on/off sequence pins. The external pull high resistor is required.
(Detected by VIN4 level good)</td></tr>
<tr><td rowspan="2">54</td><td>SUS_WARN#</td><td>$IN_{st,5v}$</td><td rowspan="2">3VSB</td><td>This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported.</td></tr>
<tr><td>TIMING_1</td><td>$OD_{12,5v}$</td><td>Active high. Timing sequence 1 of power on/off sequence pins. The external pull high resistor is required.
(Output detected by VCCOK(VDDOK) level good, ref Figure 15)</td></tr>
<tr><td rowspan="3">55</td><td>S3P5_GATE#</td><td>OD_{12}</td><td rowspan="3">3VSB</td><td>Status for S0#/S3#/S5# states application
<table><tr><th>State</th><th>S0P5_GATE#</th></tr><tr><td>S0</td><td>High level</td></tr><tr><td>S3/Deep S3</td><td>Low level /High level/*</td></tr><tr><td>S5</td><td>High level/Low level*</td></tr></table>*can be programmed*</td></tr>
<tr><td>SLOTOCC#</td><td>$IN_{st,5v}$</td><td>CPU SLOTOCC# input.</td></tr>
<tr><td>GPIO04</td><td>$OD_{12,5v}$</td><td>General Purpose IO. GPIO function is selected by register setting</td></tr>
<tr><td rowspan="3">56</td><td>S3_GATE#</td><td>OD_{12}</td><td rowspan="3">3VSB</td><td>Status for S0#/S3#/S5# states application
<table><tr><th>State</th><th>S3_GATE#</th></tr><tr><td>S0</td><td>High level</td></tr><tr><td>S3/Deep S3</td><td>Low level</td></tr><tr><td>S5</td><td>High level</td></tr></table>*can be programmed*</td></tr>
<tr><td>GPIO05</td><td>$I/OOD_{12st,5v}$</td><td>General Purpose IO. GPIO function is selected by register setting</td></tr>
<tr><td>WDTRST#</td><td>$OD_{12,5v}$</td><td>Watch dog timer signal output. WDT could be asserted via WDTRST#/PWROK/PCI_RST#.</td></tr>
<tr><td rowspan="2">62</td><td>S0P5_GATE#</td><td>$OD_{24,5v}$</td><td rowspan="2">3VSB</td><td>S0P5_Gate# for S0#/S3#/S5# states application.
<table><tr><th>State</th><th>S0P5_GATE#</th></tr><tr><td>S0</td><td>Low level</td></tr><tr><td>S3/Deep S3</td><td>High level/Low level*</td></tr><tr><td>S5</td><td>High level/Low level*</td></tr></table>*can be programmed*</td></tr>
<tr><td>GPIO13</td><td>$I/OOD_{24st,5v}$</td><td>General Purpose IO. GPIO function is selected by register setting</td></tr>
</table>

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	BEEP	OD24,5v		Beep pin.

3.3.12 Configuration Straps

Table 12 Trapping pins description

<table>
<tr><th>No</th><th>Symbol</th><th>Type</th><th>PWR</th><th>Description</th></tr>
<tr><td>5</td><td>STRAP_DPORT</td><td>IN_{t5V}</td><td>3VCC</td><td>Power on trapping (Internal pull high)
<table>
<tr><th>Strap Condition</th><th>Enable/Disable 80 Port</th></tr>
<tr><td>1(Default)</td><td>Enable 80 Port</td></tr>
<tr><td>0</td><td>Disable 80 Port</td></tr>
</table></td></tr>
<tr><td>22</td><td>FANCTL1</td><td>OOD_{12, 5V}
AOUT</td><td>3VCC</td><td>FANCTRL 1 mode select
<table>
<tr><th>Strap Condition</th><th>PWM/DAC Mode</th></tr>
<tr><td>1</td><td>PWM mode
Connect a 4.7K resistor and pull high to 3.3V</td></tr>
<tr><td>0(Default)</td><td>DAC mode</td></tr>
</table></td></tr>
<tr><td>24</td><td>FANCTL2</td><td>OOD_{12, 5V}
AOUT</td><td>3VCC</td><td>FANCTRL2 mode select
<table>
<tr><th>Strap Condition</th><th>PWM/DAC Mode</th></tr>
<tr><td>1</td><td>PWM mode
Connect a 4.7K resistor and pull high to 3.3V</td></tr>
<tr><td>0(Default)</td><td>DAC mode</td></tr>
</table></td></tr>
<tr><td>26</td><td>FANCTL3</td><td>OOD_{12, 5V}
AOUT</td><td>3VCC</td><td>FANCTRL3 mode select
<table>
<tr><th>Strap Condition</th><th>PWM/DAC Mode</th></tr>
<tr><td>1</td><td>PWM mode
Connect a 4.7K resistor and pull high to 3.3V</td></tr>
<tr><td>0(Default)</td><td>DAC mode</td></tr>
</table></td></tr>
<tr><td>78</td><td>AT_ATX_STRAP/
STRAP_TIMING</td><td>IN_{t5V}</td><td>3VSB</td><td>This pin is used to determine TIMING_EN (Index 27h[0]) and AT_ATX_MODE (Index 27h[1]) power on strap value
No internal pull up/down resister is built in, the external resistors are needed
<table>
<tr><th>Strap Condition</th><th>AMD/Intel Power Sequence</th><th>AT/ATX MODE</th></tr>
<tr><td>$3VSB \times \frac{0}{8}$</td><td>0 (Disable/Intel Mode)</td><td>0 (ATX)</td></tr>
<tr><td>$3VSB \times \frac{3}{8}$</td><td>0 (Disable/Intel Mode)</td><td>1 (AT)</td></tr>
<tr><td>$3VSB \times \frac{5}{8}$</td><td>1 (Enable/AMD Mode)</td><td>0 (ATX)</td></tr>
<tr><td>$> 3VSB \times \frac{7}{8}$</td><td>1 (Enable/AMD Mode)</td><td>1 (AT)</td></tr>
</table></td></tr>
</table>

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<table>
<tr><td>121</td><td>FAN40_100</td><td>IN_{t5V}</td><td>3VCC</td><td>Power on Fan speed
<table><tr><th>Strap Condition</th><th>40%/100% Duty</th></tr><tr><td>1(Default)</td><td>duty is 40% (PWM)</td></tr><tr><td>0</td><td>duty is 100%(PWM)</td></tr></table></td></tr>
<tr><td>122</td><td>STRAP_WDT_EN</td><td>IN_{t5V}</td><td>3VCC</td><td>Enable/Disable WDT after power
<table><tr><th>Strap Condition</th><th>Enable/Disable WDT</th></tr><tr><td>1(Default)</td><td>Disable WDT</td></tr><tr><td>0</td><td>Enable WDT</td></tr></table></td></tr>
<tr><td>124</td><td>STRAP4E_2E</td><td>IN_{t5V}</td><td>3VCC</td><td>Configuration Register I/O port
<table><tr><th>Strap Condition</th><th>I/O Port Address</th></tr><tr><td>1(Default)</td><td>4E/4F</td></tr><tr><td>0</td><td>2E/2F</td></tr></table></td></tr>
</table>

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4 Function Description

4.1 Parallel Port

The parallel port in F81768 supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP) mode. Refer to the configuration registers for more information on selecting the mode of operation.

The below content is about the Parallel Port device register descriptions. All the registers are for software porting reference.

Hardware Monitor

4.1.1 Base Address Setting

4.1.1.1 Parallel Port Data Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	DATA	R/W	00h	The output data to drive the parallel port data lines.

4.1.1.2 ECP Address FIFO Register — Base + 0

Bit	Name	R/W	Default	Description
7-0	ECP_AFIFO	R/W	00h	Access only in ECP Parallel Port Mode and the ECP_MODE programmed in the Extended Control Register is 011. The data written to this register is placed in the FIFO and tagged as an Address/RLE. It is auto transmitted by the hardware. The operation is only defined for forward direction. It divide into two parts : Bit 7 : 0: bits 6-0 are run length, indicating how many times the next byte to appear (0 = 1time, 1 = 2times, 2 = 3times and so on). 1: bits 6-0 are ECP address. Bit 6-0 : Address or RLE depends on bit 7.

4.1.1.3 Device Status Register — Base + 1

Bit	Name	R/W	Default	Description
7	BUSY_N	R	-	Inverted version of parallel port signal BUSY.
6	ACK_N	R	-	Version of parallel port signal ACK#.
5	PERROR	R	-	Version of parallel port signal PE.
4	SELECT	R	-	Version of parallel port signal SLCT.
3	ERR_N	R	-	Version of parallel port signal ERR#.
2-1	Reserved	R	11	Reserved. Return 11b when read.

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0	TMOUT	R	-	This bit is valid only in EPP mode. Return 1 when in other modes. It indicates that a 10uS time out has occurred on the EPP bus. 0: no time out error. 1: time out error occurred, write 1 to clear.

4.1.1.4 Device Control Register — Base + 2

Bit	Name	R/W	Default	Description
7-6	Reserved	-	11	Reserved. Return 11b when read.
5	DIR	R/W	0	0: the parallel port is in output mode. 1: the parallel port is in input mode. It is auto reset to 1 when in SPP mode.
4	ACKIRQ_EN	R/W	0	Enable an interrupt at the rising edge of ACK#.
3	SLIN	R/W	0	Inverted and then drives the parallel port signal SLIN#. When read, the status of inverted SLIN# is return.
2	INIT_N	R/W	0	Drives the parallel port signal INIT#. When read, the status of INIT# is return.
1	AFD	R/W	0	Inverted and then drives the parallel port signal AFD#. When read, the status of inverted AFD# is return.
0	STB	R/W	0	Inverted and then drives the parallel port signal STB#. When read, the status of inverted STB# is return.

4.1.1.5 EPP Address Register — Base + 3

Bit	Name	R/W	Default	Description
7-0	EPP_ADDR	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Address Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Address Read protocol.

4.1.1.6 EPP Data Register — Base + 4 – Base + 7

Bit	Name	R/W	Default	Description
7-0	EPP_DATA	R/W	00h	Write this register will cause the hardware to auto transmit the written data to the device with the EPP Data Write protocol. Read this register will cause the hardware to auto receive data from the device by with the EPP Data Read protocol.

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4.1.1.7 Parallel Port Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	C_FIFO	R/W	00h	Data written to this FIFO is auto transmitted by the hardware to the device by using standard parallel port protocol. It is only valid in ECP and the ECP_MODE is 010b.The operation is only for forward direction.

4.1.1.8 ECP Data FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	ECP_DFIFO	R/W	00h	Data written to this FIFO when DIR is 0 is auto transmitted by the hardware to the device by using ECP parallel port protocol. Data is auto read from device into the FIFO when DIR is 1 by the hardware by using ECP parallel port protocol. Read the FIFO will return the content to the system. It is only valid in ECP and the ECP_MODE is 011b.

4.1.1.9 ECP Test FIFO — Base + 400h

Bit	Name	R/W	Default	Description
7-0	T_FIFO	R/W	00h	Data may be read, written from system to the FIFO in any Direction. But no hardware handshake occurred on the parallel port lines. It could be used to test the empty, full and threshold of the FIFO. It is only valid in ECP and the ECP_MODE is 110b.

4.1.1.10 ECP Configuration Register A — Base + 400h

Bit	Name	R/W	Default	Description
7	IRQ_MODE	R	0	0: interrupt is ISA pulse. 1: interrupt is ISA level. Only valid in ECP and ECP_MODE is 111b.
6-4	IMPID	R	001	000: the design is 16-bit implementation. 001: the design is 8-bit implementation (default). 010: the design is 32-bit implementation. 011-111: Reserved. Only valid in ECP and ECP_MODE is 111b.
3	Reserved	-	-	Reserved.
2	BYTETRAN_N	R	1	0: when transmitting there is 1 byte waiting in the transceiver that does not affect the FIFO full condition. 1: when transmitting the state of the full bit includes the byte being transmitted. Only valid in ECP and ECP_MODE is 111b.
1-0	Reserved	R	00	Return 00 when read. Only valid in ECP and ECP_MODE is 111b.

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4.1.1.11 ECP Configuration Register B — Base + 401h

Bit	Name	R/W	Default	Description
7	COMP	R	0	0: only send uncompressed data. 1: compress data before sending. Only valid in ECP and ECP_MODE is 111b.
6	Reserved	R	1	Reserved. Return 1 when read. Only valid in ECP and ECP_MODE is 111b.
5-3	ECP_IRQ_CH	R	001	000: the interrupt selected with jumper. 001: select IRQ 7 (default). 010: select IRQ 9. 011: select IRQ 10. 100: select IRQ 11 101: select IRQ 14. 110: select IRQ 15. 111: select IRQ 5. Only valid in ECP and ECP_MODE is 111b.
2-0	ECP_DMA_CH	R	011	Return the DMA channel of ECP parallel port. Only valid in ECP and ECP_MODE is 111b.

4.1.1.12 Extended Control Register — Base + 402h

Bit	Name	R/W	Default	Description
7-5	ECP_MODE	R/W	000	000: SPP Mode. 001: PS/2 Parallel Port Mode. 010: Parallel Port Data FIFO Mode. 011: ECP Parallel Port Mode. 100: EPP Mode. 101: Reserved. 110: Test Mode. 111: Configuration Mode. Only valid in ECP.
4	ERRINTR_EN	R/W	0	0: disable the interrupt generated on the falling edge of ERR#. 1: enable the interrupt generated on the falling edge of ERR#.
3	DAMEN	R/W	0	0: disable DMA. 1: enable DMA. DMA starts when SERVICEINTR is 0.
2	SERVICEINTR	R/W	1	0: enable the following case of interrupt. DMAEN = 1: DMA mode. DMAEN = 0, DIR = 0: set to 1 whenever there are writeIntrThreshold or more bytes are free in the FIFO. DMAEN = 0, DIR = 0: set to 1 whenever there are readIntrThreshold or more bytes are valid to be read in the FIFO.
1	FIFOFULL	R	0	0: The FIFO has at least 1 free byte. 1: The FIFO is completely full.
0	FIFOEMPTY	R	0	0: The FIFO contains at least 1 byte. 1: The FIFO is completely empty.

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4.2 Hardware Monitor - Voltage

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex: 1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC/3VSB/VBAT is an exception for it is main power of the F81768. Therefore 3VCC/3VSB/VBAT can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F81768 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

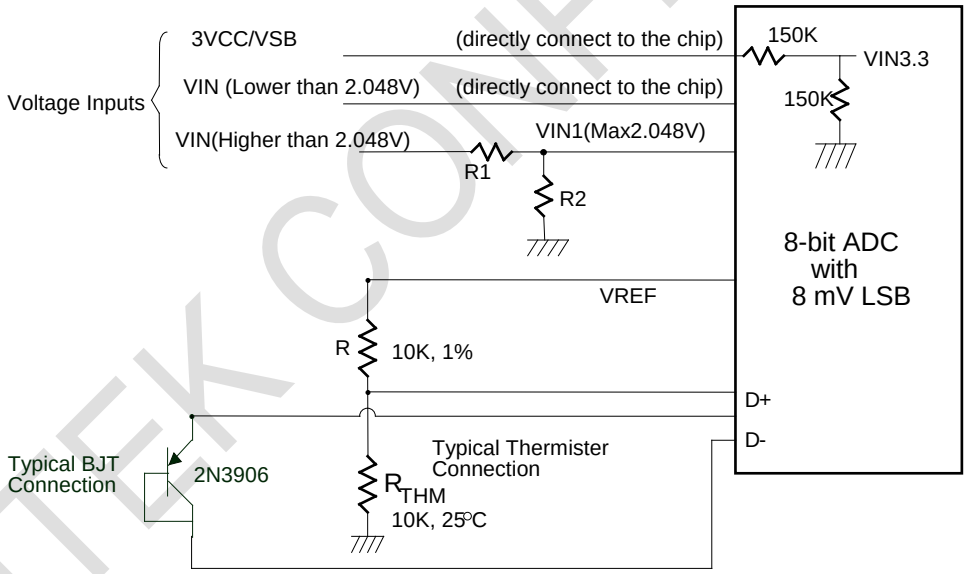
There are four voltage inputs in the F81768 and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$

Where V_{+12v} is the analog input voltage, for example:

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

Figure 3 Hardware monitor configuration



4.2.1 Over-voltage/Under-voltage Protection

F81768's **3VCC, VIN5 and VIN6** could protect the damage from voltage spikes via over voltage (OVP) and under voltage protection (UVP) function. Voltage protection function is enabled via setting the related register. When force mode occurs, the system would shut down and the system cannot be re-booted at all. Only re-plugging the power code (cut off VSB) could re-activate or re-boot the system under force mode.

4.2.2 ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency

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noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

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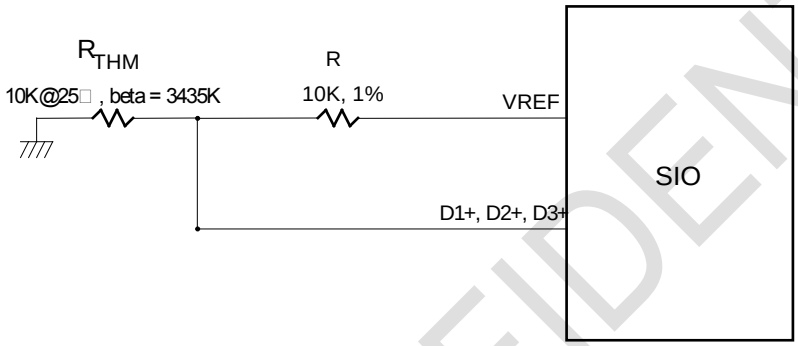
4.3 Hardware Monitor - Temperature

4.3.1 Monitor Temperature Source

4.3.1.1 Thermistor

F81768 can connect three thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) ß value is 3435K (2) resistor value is 10K ohm at 25ºC. In the Figure 3, the thermistor is connected by a serial resistor with 10K ohm, then being connected to VREF.

Figure 4 Hardware monitor configuration



4.3.1.2 Thermal Diode

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, F81768 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor from below table. In the Figure below, the transistor is directly connected into temperature pins.

Figure 5 Hardware monitor configuration

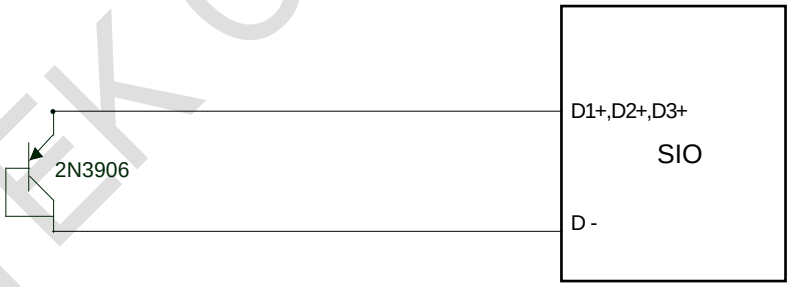


Table 13 Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

4.3.1.3 Temperature Monitor

The F81768 monitors three remote temperature sensors. These sensors can be measured from -40°C to 127°C. More detail please refers register description.

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Table 14 Display range

Display range is from -40°C to 127°C in 2's complement format

Temperature	Digital Output
-40°C	1101 1000
-1°C	1111 1111
1°C	0000 0001
90°C	0101 1010
127°C	1111 1111
Open	1000 0000

4.3.1.4 Intel PECI

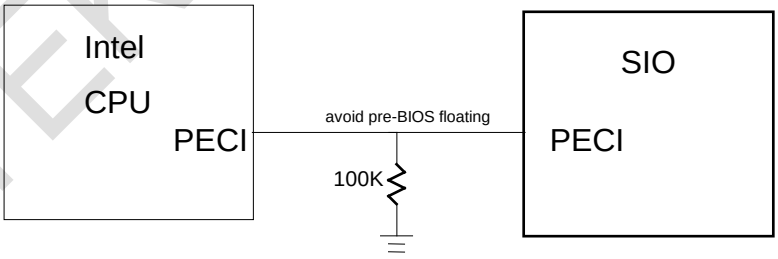
F81768 support Intel PECI1.1/PECI3.0 interfaces to read temperature from PECI device.

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked on-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or login '1'. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

F81768 can connect to CPU & read the temperature data from CPU directly. Then the fan control machine ofF81768 can implement the fan to cool down CPU temperature. The application circuit is as below.

Figure 6 INTEL PECI typical application



The F81768 integrated most of PECI 3.0 commands for the future advantage application. More detail, please refer to the register descriptions.

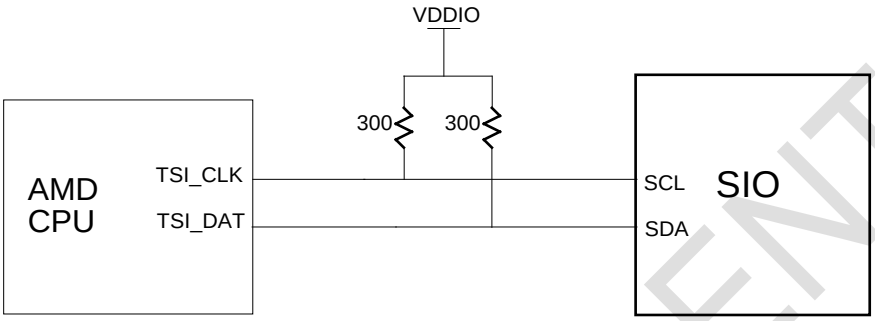
4.3.1.5 AMD TSI

TheF81768 provides AMD Temperature Sensor Interface (TSI) interfaces for new generational CPU temperature sensing. In this interface, there are SIC and SID signals for temperature information reading from AMD CPU. The SIC signal is for clocking use, the other is for data transferring. More detail, please refer register description.

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The TSI is a simple SMBUS master to communicate with AMD CPU or Intel CPU to getting the temperature of CPU. It supports byte sending, byte receiving, read/write byte, read/write block and quick command of SMBus protocol. When power on the hardware automatically fetch the temperature use the protocol per the specification of AMD/Intel. User can use the provided registers to control the SCL/SDA as a SMBus master. The SCL signal is for clocking use, the SDA is for data transferring.

Figure 7 AMD TSI typical applications



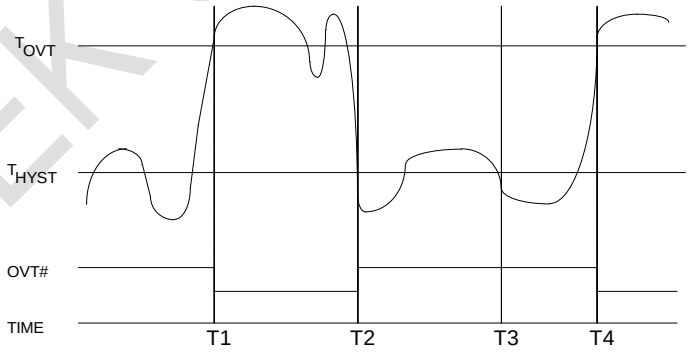
4.3.2 Temperature Interrupt Detection

4.3.2.1 Over Temperature Signal (OVT#)

There is a hysteresis mode of OVT# functions, and refers t1 to t4 temperature in below figure which Sensor ($\mathbf{T_{OVT}}$) detects temperature exceeds the high threshold limit value and triggers the OVT# when time arrives t1. Time t2, OVT# be asserted until the temperature goes below the hysteresis temperature ($\mathbf{T_{HYST}}$).

Figure 8 Temperature OVT# Signal

T_{OVT} : OVER Temperature Threshold
T_{HYST}: Hysteresis Temperature



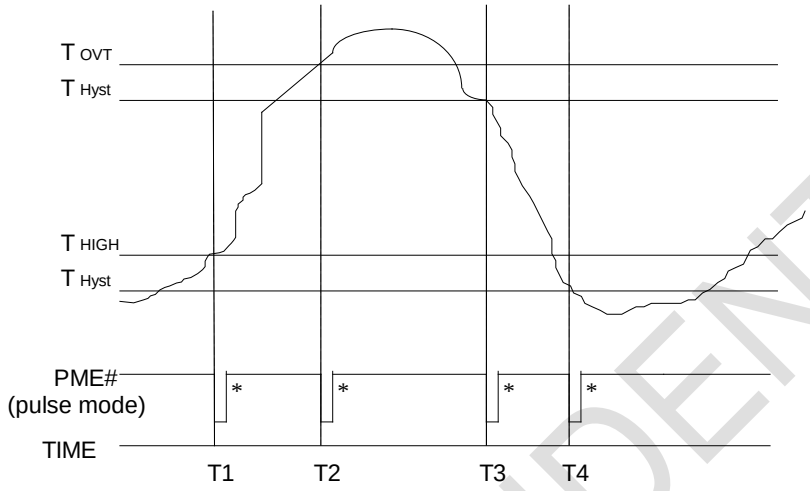
4.3.2.2 Power Management Event (PME#)

Power Management Event (PME#) interrupt for temperature is shown as Figure 8. Temperature exceeding $\mathbf{T_{HIGH}}$ (High Limit Threshold) and $\mathbf{T_{OVT}}$ (OVT Threshold), or going below $\mathbf{T_{HYST}}$ (High Hysteresis and Low Hysteresis) will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register.

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Figure 9 Hysteresis mode illustrations

T_{OVT} : Over Temperature Threshold
T_{HYST}: Hysteresis Temperature
T_{HIGH}: High Limit Threshold
**: Interrupt Reset when Interrupt Status Registers are written*



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4.4 Hardware Monitor – Fan Controller

4.4.1 Fan Speed Count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

As the register description of datasheet, the parameter “Count” register provides 12-bit resolution for RPM counting. In Fintek design, the value of parameter “Count” is from 4096 ~ 64 (5 bit filter). Therefore the RPM measure capability is from 366 ~ 23438 rpm.
Above example is for 2 pulses tachometer (Normal 4 Phases fan) output per round. If you use 8 Phases fan, means output 4 pulses per round. The RPM measure capability is from 183 ~ 11719 rpm.

4.4.2 Fan Speed Control

The F81768 provides 2 fan speed control methods: one is DAC FAN control and the other is PWM duty cycle.

4.4.2.1 DAC Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output_voltage (V)} = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

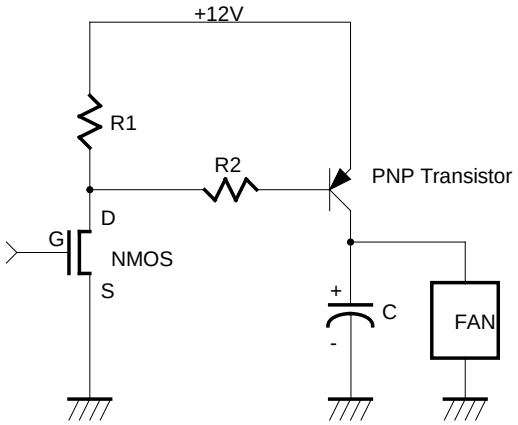
4.4.2.2 PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

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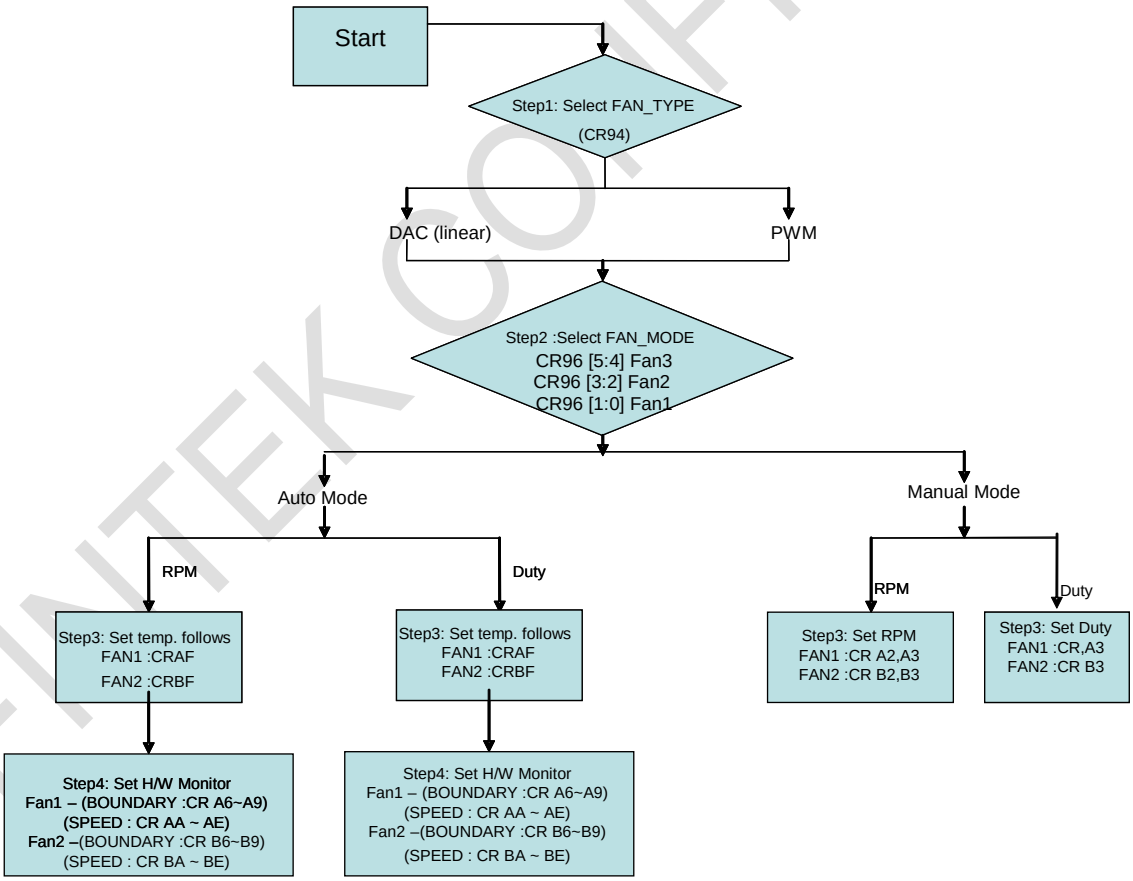
Figure 10 +12/5V PWM fan control application circuit



4.4.3 Fan Speed Control Mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode 3. Linear auto mode. Please refer to the figure below. For more detail, please refer the description of registers.

Figure 11 Fan type and mode selection flow



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4.4.3.1 Manual mode

For manual mode, it generally acts as software fan speed control.

4.4.3.2 Auto mode

In auto mode, the F81768 provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F81768 can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE. And the hysteresis setting (0 ~ 15°C) could also be found in register 0x98.

The Manual Mode and Auto Mode could be selected by register 0x96h.

There are two kinds of auto mode: stage auto mode and linear auto mode. The “FAN1_INTERPOLATION_EN” in register 0xAFh is used for linear auto mode enable. The following examples explain the differences for stage auto mode and linear auto mode.

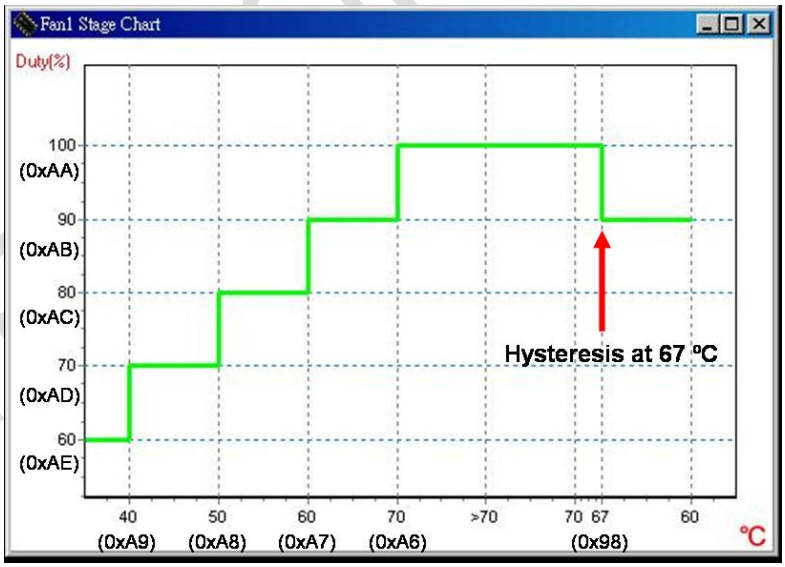
4.4.3.3 Stage auto mode

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting: PWM Duty and RPM %.

A. Stage auto mode (PWM Duty)

Set the temperature limits as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

Figure 12 Stage mode fan control illustration



a. Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.

b. Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.

c. For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.

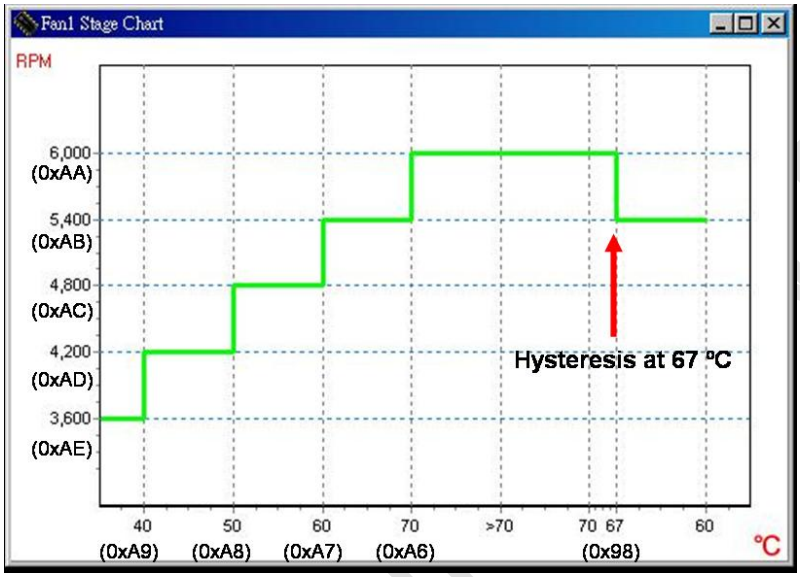
d. If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would reduce to 90% PWM duty.

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B. Stage auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 5,400 rpm, 4,800 rpm, 4,200 rpm, and 3,600 rpm (assume the Max Fan Speed is 6,000 rpm).

Figure 13 Stage mode fan control illustration



a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 rpm (60% of full speed).

b. Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 rpm to 5,400 rpm and increasing with the temperature level.

c. For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 rpm.

d. If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 rpm.

4.4.3.4 Linear auto mode

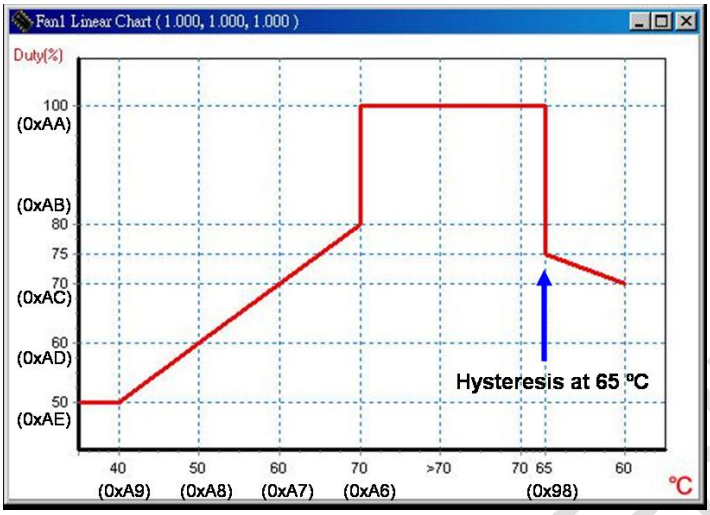
F81768 also supports linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

A. Linear auto mode (PWM Duty)

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

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Figure 14 Linear mode fan control illustration-1



a. Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty

b. Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the tempreature variation. The temp.-fan speed monitoring flash interval is 1sec.

c. Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).

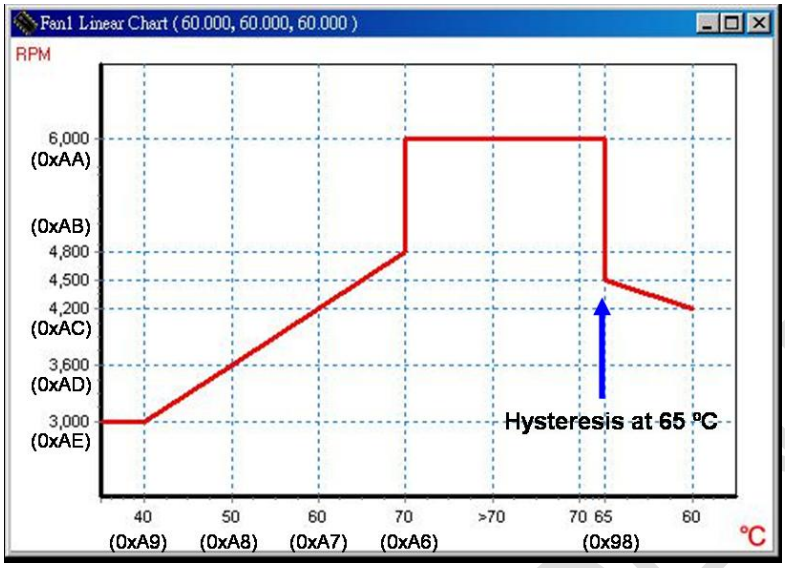
d. If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

B. Linear auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 rpm, 4,800 rpm, 4,200 rpm, 3,600 rpm and 3,000 rpm (assume the Max Fan Speed is 6,000 rpm).

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Figure 15 Linear mode fan control illustration



a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 rpm (50% of full speed).

b. Once the temperature is over 40°C,50°C and 60°C, the fan speed will vary from 3,000 to 4,800 rpm almost linearly with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.

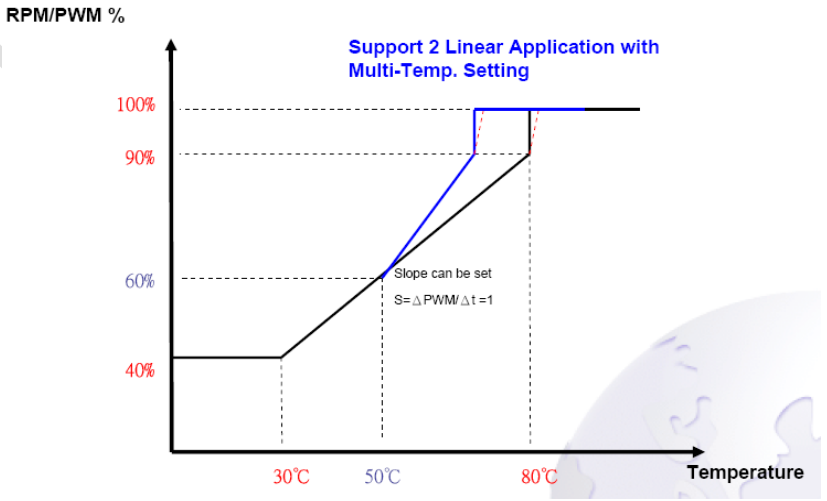
c. Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 rpm.

d. If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed wull reduce from full speed and decrease linearly with the temperature.

4.4.4 Fan Speed Control with Multi-temperature.

F81768 supports Multi-temperature for one fan control. This function works with linear auto mode can extend two linear slopes for one Fan control. As the graph below, this machine can support more silence fan control in low temperature environment and faster fan speed in high temperature segment. More detail setting please refers to the registers.

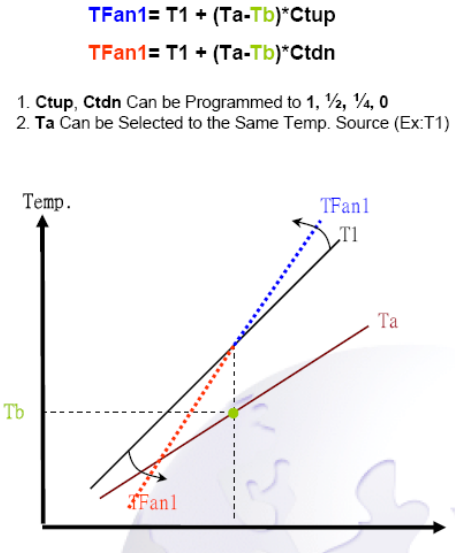
Figure 16 Multi-Temperature Graph



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In the figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.

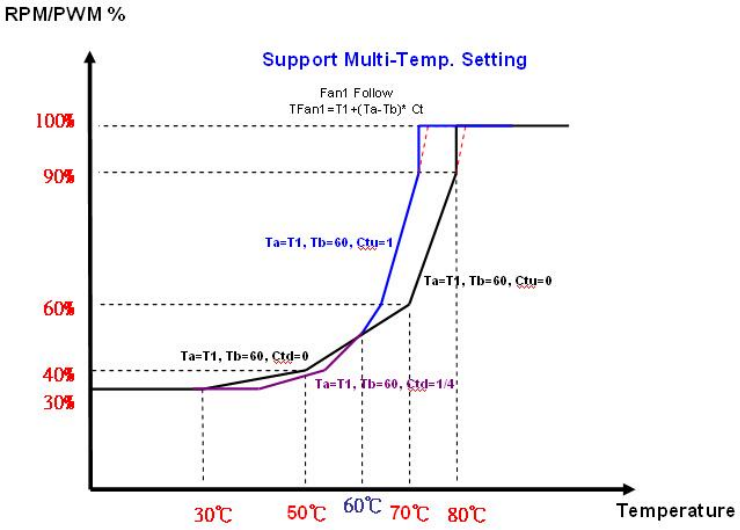
Figure 17 Multi-Temperature Graph



In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

Figure 18 Multi-Temperature Graph

EX: Ta = T1, Tb = 60, Ctu = 1, Ctd = 1/4



4.4.5 FAN_FAULT#

4.4.5.1 Condition

FAN_FAULT# (SIO Internal Signal) will be asserted when the fan speed doesn't meet the expected fan speed within a

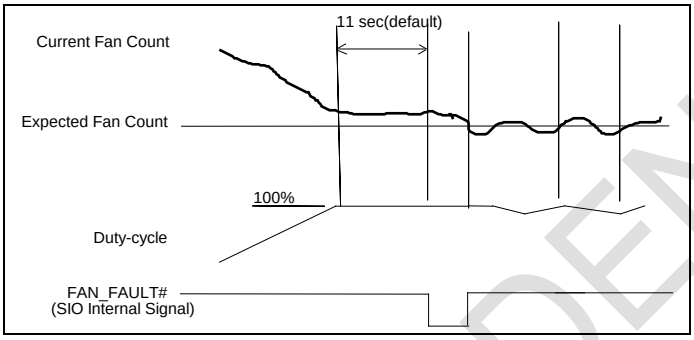
programmable period (default is 11 seconds, can be set in Index 9Fh[3:0]) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may issue the FAN_FAULT# event.

Related registers: FAN Interrupt Status 91h[2:0], FAN Real Time Status 92h[2:0]

Condition 1: The fan speed count can't reach the fan expected count in time when PWM_DUTY reaches 0xFF

For instance, set the fan expectation speed as 10,000 rpm, but the limit speed of the fan mechanism is 5,000 rpm. When fan start, FAN_FAULT# condition will be satisfied after 11 seconds.

Figure 19 FAN_FAULT# Event



Condition 2: Fan does not rotate

For instance, the fan duty is bigger than start up duty cycle (FANx_STOP_DUTY) when system boot up. At meantime, the fan count value is 0xFFF. So the FAN_FAULT# condition will be satisfied.

4.4.5.2 Asserting configuration

The BEEP and PME# are the asserting interface of FAN_FAULT# supported on the SIO.

Table 15 FAN_FAULT# Asserting Configuration

	FAN BEEP Enable	FAN PME# Enable
FAN_FAULT#	Index 93h[2:0]	Index 90h[2:0]

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4.5 ACPI

4.5.1 ACPI General Conception

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

ACPI includes three sub items as below:

1	Power Control Include: – Wake up stage detection – AC loss & resume control methods
2	EU Power Saving Function (EUP/ERP Command Lot 6.0)
3	Power Saving Mode Intel Power Saving Function (Deep Sleep Well, DSWl) and G3 Like Function

Where item 2 & 3 could be coexisted via ERP_CTRL0# (follow SLP_SUS#) & ERP_CTRL1# (After the system enters S3 1.024s & S5 6.4s, EUP/ERP mode could be achieved).

Before entering into the main section, let's check out the related hardware control signal first.

Control Signal	Power On/Off Control (AC Resume)	Power Management Event	Wake up	Intel DSW Hand Shaking	EUP/ERP Control
RSMRST#	◇				
S3#	◇				
S5#	◇				
PSIN#	◇				
PSOUT#	◇		☆★		
ATXPG_IN	◇				
PS_ON#	◇				
PWROK	◇				
PME#		◇	☆★		
PS/2 KB/MS			☆★		
RI1#/RI2#			☆★		
GPIO1x/3x/4x/5x			☆★		
SLP_SUS#				◇	

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Control Signal	Power On/Off Control (AC Resume)	Power Management Event	Wake up	Intel DSW Hand Shaking	EUP/ERP Control
SUS_ACK#				◇	
SUS_WARN#				◇	
ERP_CTRL0#				◇	◇
ERP_CTRL1#					◇

◇: Supported
★: Wake up via ERP
☆: Wake up via System Power Control

4.5.2 Wake Up Stage Detection

F81768 is counted on the chipset SLP_S3#, SLP_S4#/SLP_S5# stage, to decide the wake up stage as below:

Table 16 True table of IO state referring to platform power state

ACPI Stage	SLP_S3#	SLP_S4# /SLP_S5#
S0	High	High
S3	Low	High
S5	Low	Low

Power saving mode would be activated via CR0A index E0 bit 7.

When the system is at the normal sleep state (S3, S4, S5) or deep sleep (G3') state, F81768 could wake up via PWSOUT# & PME#. See below for the related registers:

Table 17 Wake up by PME# of related setting

Wake up by PME#	Index 2Dh	CR0A Index E0h, E8h	CR0A Index F0~F3h
Normal Sleep State	✓Support		✓Support
Power Saving State	✓Support	✓Support	

Table 18 Wake up by PWSOUT# of related setting

Wake up by PWSOUT#	Index 2Dh	CR 0A Index 30h	CR0A Index E0h, E8h	CR0A Index F4h
Normal Sleep State	✓Support	✓Support		✓Support
Power Saving State	✓Support	✓Support	✓Support	

4.5.3 AC Loss & Resume Control Methods

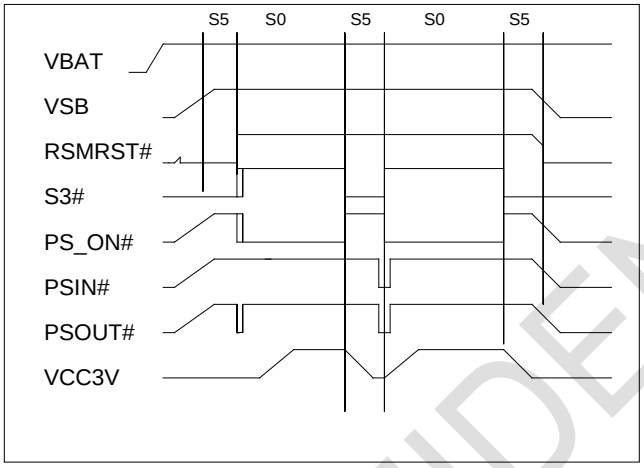
There are 5 modes under power loss state via setting ACPI control register, and they are Always On, Always Off, Bypass Mode, Keep Last State Mode 1 and Keep Last State Mode 2.

In Keep Last State Mode 1, one register will latch the status before power loss. If it is power on before power loss, it will automatically power on when power is resumed. If it is power off before power loss, it will remain power off when power is resumed. See below for the detail:

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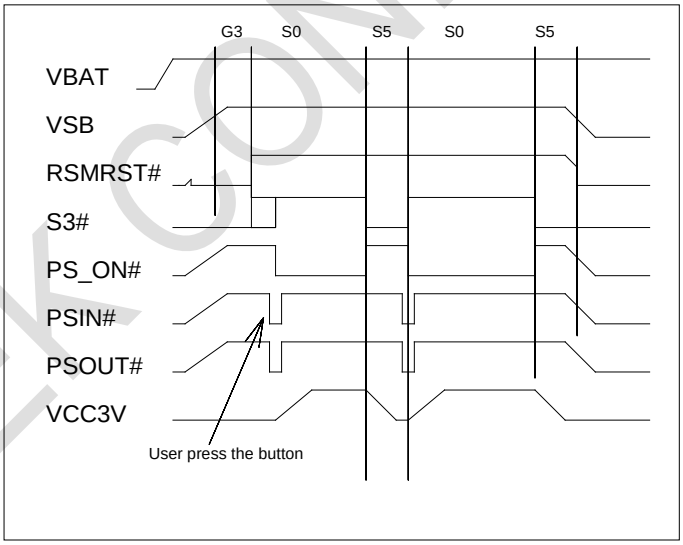
4.5.3.1 Always on (S0)

When AC resume, the system will power on automatically (send a PWSOUT# low pulse and then sinking the PS_ON# low). See below for the timing:



4.5.3.2 Always off (S5)

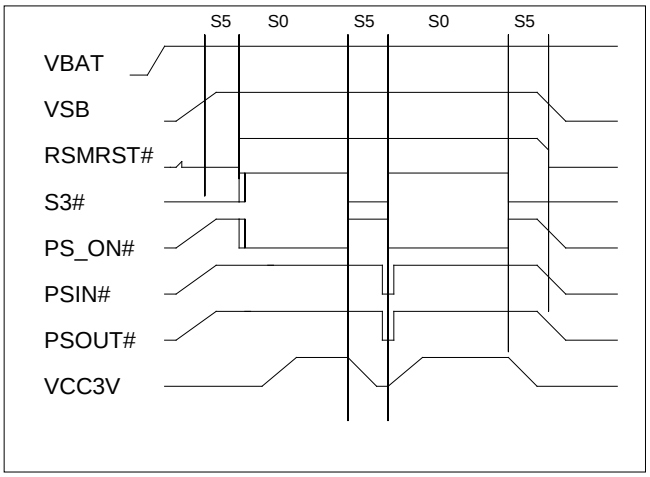
When AC resume, the system is in off state and waiting for the wakeup events. See below for the timing:



4.5.3.3 Bypass (follow the chipset after G3 stage)

When AC resume, inverting the S3 signal to PS_ON#. See below for the timing:

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4.5.3.4 Keep Last State Mode

Using ATXPG_IN, VCC (PWROK), VSB (RSMRST) and S3 signals to detect the sleep state while AC loss occurs. One of the signal (ATXPG_IN, VCC or VSB under 2.8V) sinks low, SIO will latch the S3 signal to decide the system to be at “always on” or “always off” mode. See below table:

Signal / AC loss state	ATXPG	VCC	VSB	AC resume
AC loss in S0/S1 (S3=1)	↓	↓	↓	Always on
AC loss in S3/S4/S5 (S3=0)	↓	↓	↓	Always off

4.5.3.5 Keep Last State Mode New Mode

Using VCC (PWROK), VSB (RSMRST) and S3 signals to detect the sleep state while AC loss occurs.

SIO will latch the S3 signal status before AC loss, according this status to decide the system to be at “always on” or “always off” mode. See below table:

Signal / AC loss state	VCC	VSB	AC resume
AC loss in S0/S1 (S3=1)	↓	↓	Always on
AC loss in S3/S4/S5 (S3=0)	↓	↓	Always off

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4.5.4 Power Saving

In order to achieve the lower power consumption, the ERP_CTRL# could also turn off the 3VA so that the system can enter the Fintek G3' state.

The F81768 supports Intel Chipset timing. There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWROK.

4.5.4.1 ErP Mode Select

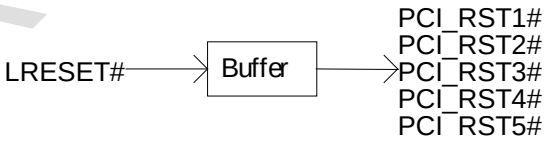
ERP_CTRL0# and ERP_CTRL1# control the standby power rail on/off to fulfill the purpose which decreases the power consumption when the system in the sleep state or the soft-off state. Those two pins connected to the external PMOSs with default values are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, those two pins can be programmable to set which power rail is turned on. The programmable register is powered by battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3-like state), the F71878 consumes 5VSB power rail only to realize a low power consumption system.

Fintek provides 2 ErP modes, and they are Fintek G3' mode, Intel DSW mode. The register for setting this mode is at CR0A, Index EC [7:6].

Bit	Name	Description
7-6	ERP_MODE	00: Fintek G3' mode. 01: Intel DSW + Fintek G3` mode. 10: Reserved. 11: Intel DSW mode.

4.5.5 PCI Reset

The F81768 supports 5 output buffers for 5 reset signals.



So far as the PWROK issue is as the Figure above. PWROK are gated with VDD3VOK, ATXPG and S3#I. PWROK is delayed 400ms (Default) as VCC arrives 2.8V, and the delay timing can be programmed by register. An additional programmable delay could be added to PWROK (0ms, 100ms, 200ms and 400ms). If RSTCON# and PCI_RST4#/PCI_RST5# are enabled, RSTCON# could be programmed to be asserted via PWROK or PCI_RST4#/PCI_RST5#.

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4.5.6 Power OK

Figure 20 Intel mode PWROK logic sequence

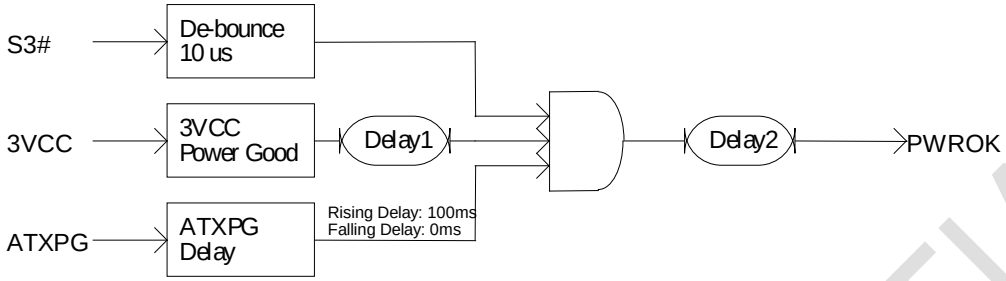
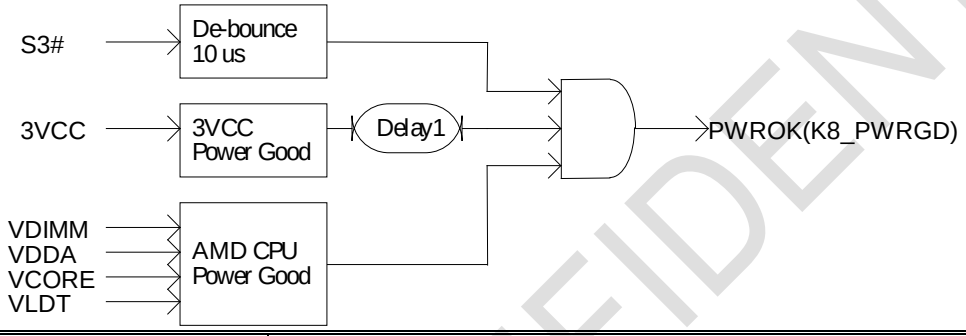


Figure 21 AMD mode PWROK logic sequence



Delay	LDN 0x0A Index F5h	Description
Delay 1	VDD_DELAY	Bit [4-3]:The PWROK delay timing from 3VCCOK by followed setting 200ms (default)
Delay 2	PWROK_DELAY	Bit [7-6]: The additional PWROK delay. 200ms (default)

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4.5.6.1 PWROK Control Signal

PWROK are gated with VDD3VOK, ATXPG and S3#. PWROK is delayed 400ms (Default) when VCC arrives 2.8V, and the delay timing can be programmed by register. An additional programmable delay could be added to PWROK (0ms, 100ms, 200ms and 400ms). It can be set in the register 0x0AF5.

Figure 22 Intel & AMD Mode PWROK Logic Sequence

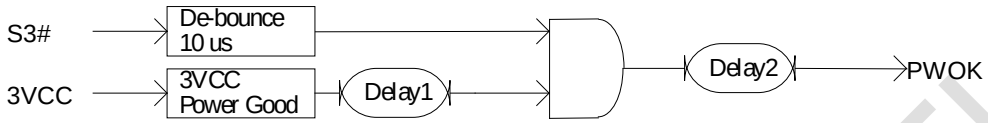


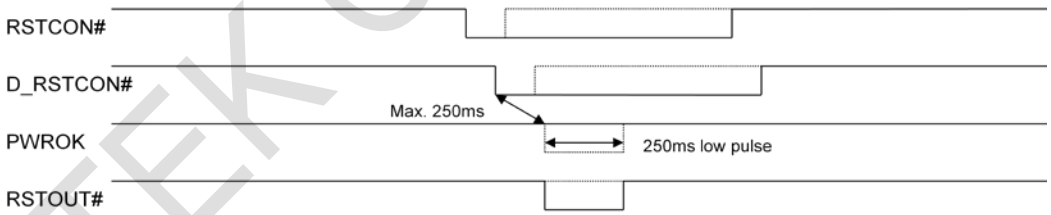
Table PWROK register setting guide

Delay	LDN 0x0A Index F5h	Description
Delay 1	VDD_DELAY	Bit [4-3]:The PWROK delay timing from 3VCCOK by followed setting 200ms (default)
Delay 2	PWROK_DELAY	Bit [7-6]: The additional PWROK delay. 200ms (default)

4.5.6.2 RSTCON# and RSTOUT# Function

F81768 has the RSTCON# / RSTOUT# function to reset the system. The function could be enabled in the register 0xF7 bit0 RSTOUT_EN. To enable this function, pin59 PCI_RST4# would change to the RSTOUT# and the pin61 RSTCON# would change to the RSTCON# function. Refer to the following Figure, we can choose whether PWROK or RSTOUT# would follow the RSTCON# low pulse and assert a 250 ms low pulse in register 0xF5 bit5. Also if the function is enabled, PCI_RST4# would not follow the LRESET# and PCI_RST5# would not follow the RSTCON# signal.

Figure 23 RSTCON and RSTOUR



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4.6 AMD Power Timing Control Sequence

The F81768 offers 4 timing pins which are designed for AMD platform power sequence control including VDIMM, VDDA, Vcore, and VLDT (default) or other timing application purposes. All the timings on/off are relative to S3#/S5# and can be programmed by the register 0x0AF7. As shown in the below Figure, the default timings of TIMING_1~4 are displayed in below figure, and all the timings are enabled in the S0 state except TIMING_1. However, TIMING_2~4 can be programmed to enable in the S3 state, and TIMING_1 can also be programmed to disable in the S3 state.

Figure 24 AMD power sequence from S0 to S5

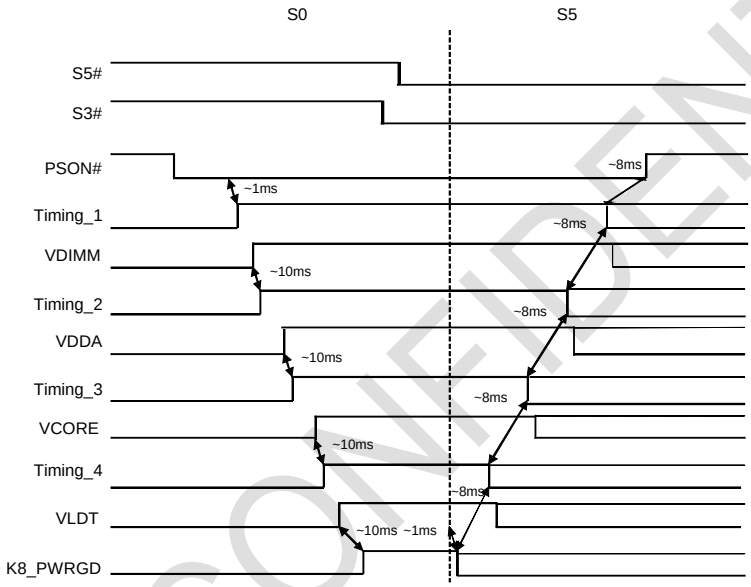
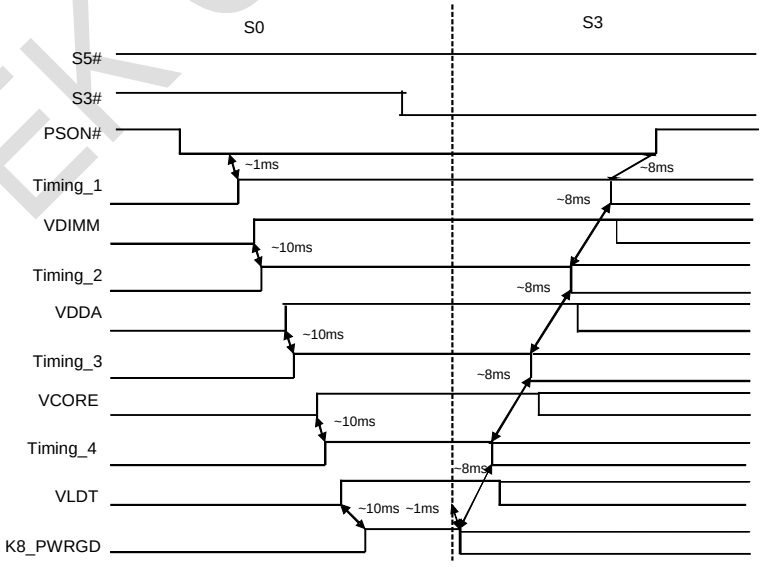


Figure 25 AMD power sequence from S0 to S3



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4.7 Power Control

4.7.1 Gate Control

There are 3 timing switching pins which are named as S3_GATE#, S3P5_GATE# and S0P5_GATE#. They can be applied in the certain applications about power switch which depends on the ACPI states. The detail timing can be referred in the following diagrams. The default timing of S0P5_GATE# in the S5 state is low, but it can be programmed high by the register 0x0AF6.

Figure 26 Gate control timing chart-1

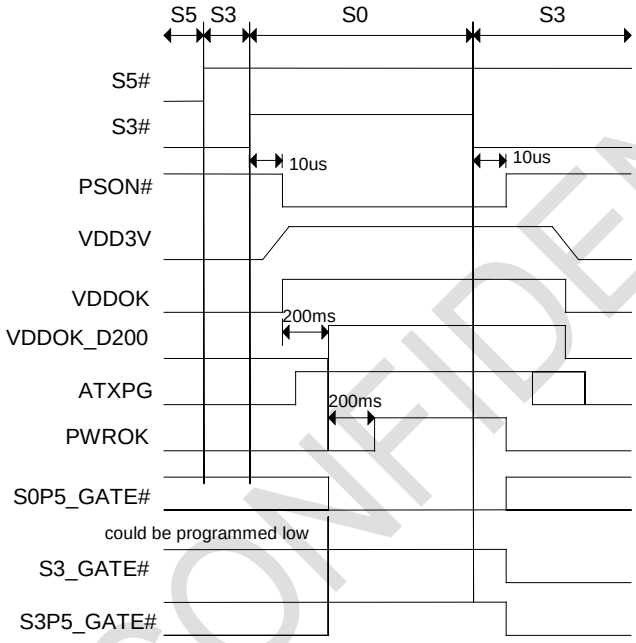
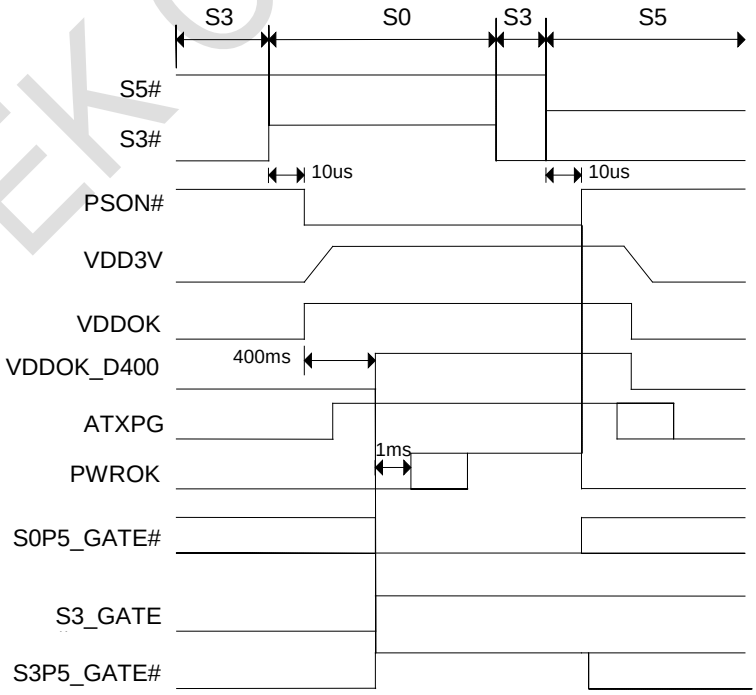


Figure 27 Gate control timing chart-2



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Table 19 Gate control table

	S0	S3/Deep S3	S5
S3_GATE#	High	Low	High
S0P5_GATE#	Low	High/Low*	High/Low*
S3P5_GATE#	High	Low/High*	High/Low*

** = Programmable*

4.7.2 PSIN# Detect

The purpose of PSIN# detecting flag is to detect the PSIN# exceeds the defined time or not. If exceeds the defined time, it could set a flag for BIOS usage. See below figures for detail:

Figure 28 Typical turn on Sequence

When the system is booting from S3/S4/S5 to S0, the typical sequence is send PSIN# pulse to PSOUT#. When the system is off from S0 to S3/S4/S5, 3VCC will be low after sends PSIN# pluse to PSOUT#.

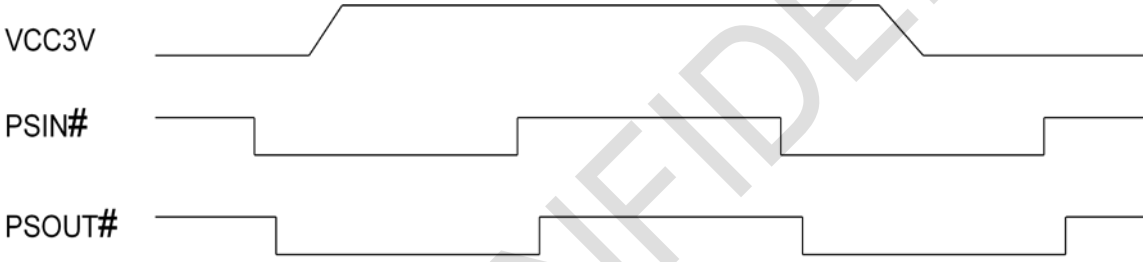


Figure 29 PSIN# Flag turn on detecting sequence

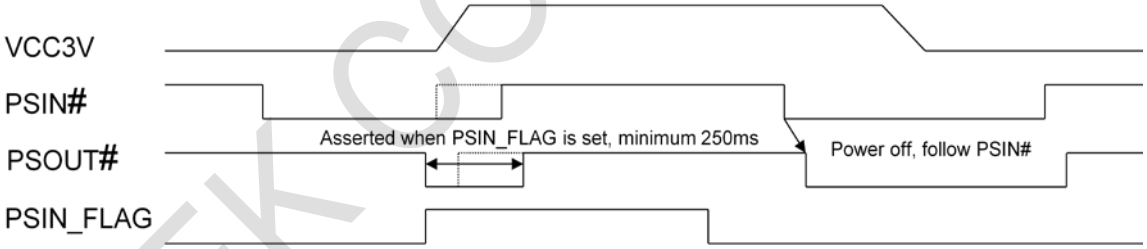
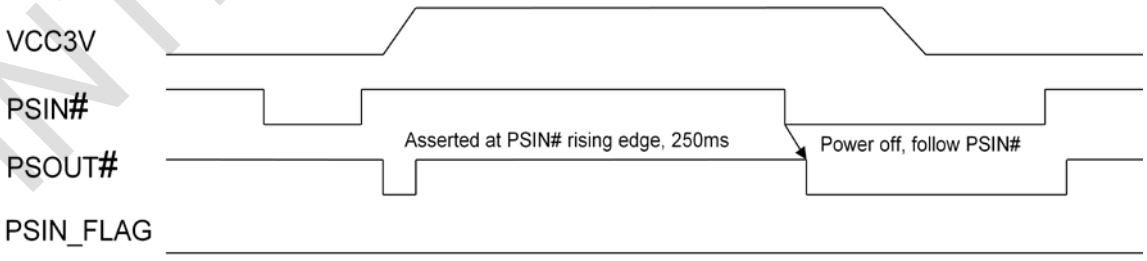


Figure 30 PSIN# Flag turn on detecting exceptional circumstance

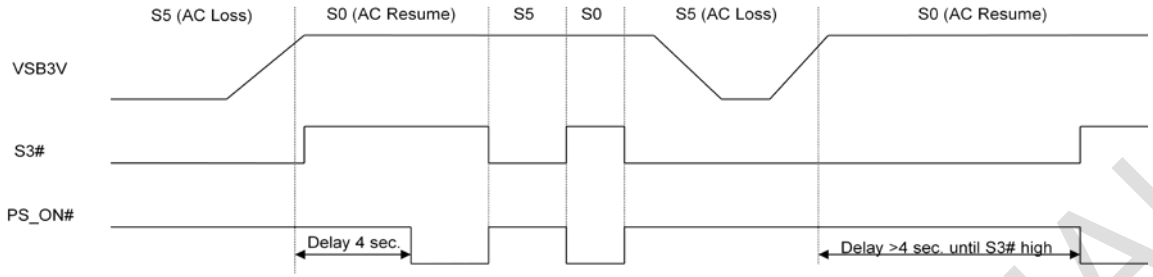


4.7.3 Power-on Delay Function

The purpose of power-on delay 4 seconds function is protecting some PC cannot turn-on after AC resume. See the related register for the power on delay 4 seconds (Index 28[7]).

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Figure 31 Delay Function



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4.8 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60h. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60h or 64h. Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

Status Register

The status register is an 8-bit read-only register at I/O address 64h that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

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4.8.1 Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Return 55h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high
8’h03: indicate keyboard data is low
8’h04: indicate keyboard data is high</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>C8h</td><td>Enable Keyboard/Mouse swap.</td></tr>
<tr><td>C9h</td><td>Disable Keyboard/Mouse swap.</td></tr>
<tr><td>CAh</td><td>Read the data written by CBh command.</td></tr>
<tr><td>CBh</td><td>Written a scratch data. This byte could be read by CAh command.</td></tr>
</table>

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D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Low pulse on KBRST# about 6μS

4.8.2 PS/2 wakeup function

The KBC supports keyboard and mouse wakeup function. KBC will assert PME or PSOUT# signal. Those wakeup conditions are controlled by the configuration register.

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4.9 General-Purpose I/O (GPIO) Ports

F81768 has 64 pins GPIO in total. All GPIO supports Input/Output control, Output data control, input status and Open Drain/Push Pull function selection. The GPIO0X, 1X, 3X, 4X, 5X, 6X support SMI interrupt status.

The GPIO6x supports the scan code function, please see registers for detail.

4.9.1 GPIO Access Method

There are nine sets of GPIO in F81768 which can be accessed by three ways as below:

1. Configuration register port: Use 0x4E/0x4F (or 0x2E/0x2F) port with logic device number 0x06. Please refer to configuration register for detail.
2. Index/Data port: The index port is base address + 0 and data port is base address + 1. To access the GPIO register, user should first write index to index port and then read/write from/to data port. The index for each register is same as the definition in configuration register.
3. Digital I/O: This way could access GPIO data register only. It is used for quickly control the GPIO pins. The register for each address is as list:

4.9.2 Scan Code Function

F81768 has 8 GPIO pins (GPIO 60~67) support scan code. These pins can not only set the volume up/down, mute and PWM up/down but also any function keys on keyboard. The protocol for these pins is scan code, so we don't need a driver to connect this function at OS. F81768 provides the programmable combination key as Clt+Alt+code for GPIO64~67. If the button for the GPIO has been pressed continuously over nearly 1 second (delay time), the GPIO will repeatedly sending this function in an interval of 50 ms (repeat time). The delay time could be set from 0.5 to 1.5 sec. The repeat time could be set from 50, 100, 250 to 500 ms.

4.9.3 GPIO0x

- Z means high impendence.
- If the external circuit is pull high then the pin status is "H"; else if the external circuit is pull low then the pin status is "L".
- "User define" means by programming the configuration register.

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
49	GPIO00	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
50	GPIO01	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
51	GPIO02	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
52	GPIO03	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
55	GPIO04	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
56	GPIO05	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
57	GPIO06	Z/User define	User define	User define	User define	VBAT	3VA/VBAT	3VA
104	GPIO07	Z	User define	Z	Z	3VA	LRESET#	3VCC

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4.9.4 GPIO1x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
59	GPIO10	Z	User define	User define	User define	3VA	3VA	3VA
60	GPIO11	Z	User define	User define	User define	3VA	3VA	3VA
61	GPIO12	Z	User define	User define	User define	3VA	3VA	3VA
62	GPIO13	Z	User define	User define	User define	3VA	3VA	3VA
63	GPIO14	Z	User define	User define	User define	3VA	3VA	3VA
64	GPIO15	Z	User define	User define	User define	3VA	3VA	3VA
65	GPIO16	Z	User define	User define	User define	3VA	3VA	3VA
66	GPIO17	Z	User define	User define	User define	3VA	3VA	3VA

4.9.5 GPIO2x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
126	GPIO20	Z	User define	Z	Z	3VA	LRESET#	3VCC
127	GPIO21	Z	User define	Z	Z	3VA	LRESET#	3VCC
128	GPIO22	Z	User define	Z	Z	3VA	LRESET#	3VCC
1	GPIO23	Z	User define	Z	Z	3VA	LRESET#	3VCC
2	GPIO24	Z	User define	Z	Z	3VA	LRESET#	3VCC
3	GPIO25	Z	User define	Z	Z	3VA	LRESET#	3VCC
5	GPIO26	Z	User define	Z	Z	3VA	LRESET#	3VCC
6	GPIO27	Z	User define	Z	Z	3VA	LRESET#	3VCC

4.9.6 GPIO3x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
7	GPIO30	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
8	GPIO31	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
9	GPIO32	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
10	GPIO33	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
11	GPIO34	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
12	GPIO35	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
13	GPIO36	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA
14	GPIO37	Z/User define	User define	User define	User define	3VA	3VA/VBAT*	3VA

*Reset signal is selectable

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4.9.7 GPIO4x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
25	GPIO40	Z	User define	Z	Z	3VA	LRESET#*	3VCC
26	GPIO41	Z	User define	Z	Z	3VA	LRESET#	3VCC
27	GPIO42	Z	User define	Z	Z	3VA	LRESET#	3VCC
28	GPIO43	Z	User define	Z	Z	3VA	LRESET#	3VCC
84	GPIO44	Z	User define	User define	User define	3VA	3VA	3VA
80	GPIO45	Z	User define	User define	User define	3VA	3VA	3VA
81	GPIO46	Z	User define	User define	User define	3VA	3VA	3VA
83	GPIO47	Z	User define	User define	User define	3VA	3VA	3VA

4.9.8 GPIO5x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
15	GPIO50	Z/User define	User define	User define	User define	3VA	3VA/VBAT	3VA
16	GPIO51	Z/User define	User define	User define	User define	3VA	3VA/VBAT	3VA
17	GPIO52	Z/User define	User define	User define	User define	3VA	3VA/VBAT	3VA
18	GPIO53	Z/User define	User define	User define	User define	3VA	3VA/VBAT	3VA
19	GPIO54	Z/User define	User define	User define	User define	3VA	3VA/VBAT	3VA

4.9.9 GPIO6x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
100	GPIO60	Z	User define	Z	Z	3VA	LRESET#*	3VCC
101	GPIO61	Z	User define	Z	Z	3VA	LRESET#	3VCC
102	GPIO62	Z	User define	Z	Z	3VA	LRESET#	3VCC
103	GPIO63	Z	User define	Z	Z	3VA	LRESET#	3VCC
105	GPIO64	Z	User define	Z	Z	3VA	LRESET#	3VCC
106	GPIO65	Z	User define	Z	Z	3VA	LRESET#	3VCC
107	GPIO66	Z	User define	Z	Z	3VA	LRESET#	3VCC
108	GPIO67	Z	User define	Z	Z	3VA	LRESET#	3VCC

4.9.10 GPIO7x

Pin	Name	PIN Status				Register Power Well	Register Reset Signal	Pin Power Well
		G3 → S5	S0	S3	S5			
109	GPIO70	Z	User define	Z	Z	3VA	LRESET#*	3VCC

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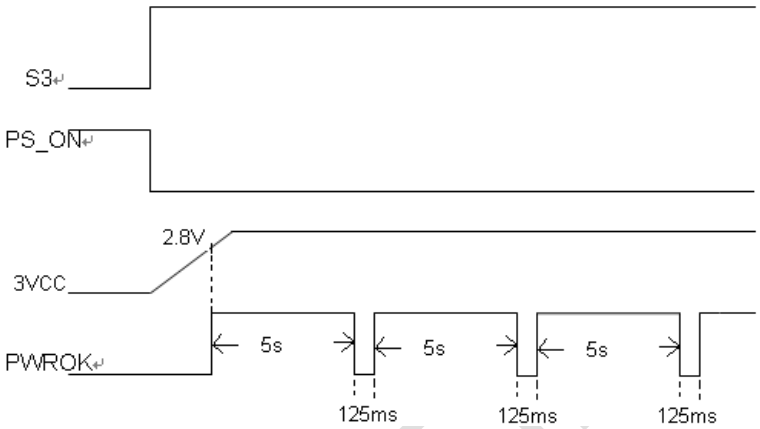
110	GPIO71	Z	User define	Z	Z	3VA	LRESET#	3VCC
111	GPIO72	Z	User define	Z	Z	3VA	LRESET#	3VCC
112	GPIO73	Z	User define	Z	Z	3VA	LRESET#	3VCC
113	GPIO74	Z	User define	Z	Z	3VA	LRESET#	3VCC
114	GPIO75	Z	User define	Z	Z	3VA	LRESET#	3VCC
115	GPIO76	Z	User define	Z	Z	3VA	LRESET#	3VCC
116	GPIO77	Z	User define	Z	Z	3VA	LRESET#	3VCC

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4.10 Watchdog Timer Function

Watch dog timer is provided for system controlling. If time-out can trigger one signal to high/low level/pulse, the signal is depend on register setting. The time unit has two ways 1sec or 60sec. In pulse mode, there are four pulse widths can be selected (1ms/25ms/125ms/5sec). Please refer the device register description as below.

Table 20 WDT pulse mode behavior



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5 Configuration Registers

5.1 Overview

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

"-" Reserved or Tri-State

Table 21 Global Control Registers

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	-
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register 1	0	0	0	1	0	0	1	0
21	Chip ID Register 2	0	0	0	1	0	0	0	0
23	Vendor ID Register 1	0	0	0	1	1	0	0	1
24	Vendor ID Register 2	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	-	-	0	0	0	-
26	Clock Select Register	0	-	0	-	0	0	0	0
27	Configuration Port Select Register	1	0	0	-	0	0	0	0
28	TSI Level Select Register (FUNC_PROG_SEL = 0)	1	1	1	0	0	0	0	0
29	TSI Pin Select Register (FUNC_PROG_SEL = 1)	0	0	0	0	0	0	0	0
29	Multi Function Select 1 Register	0	1	1	0	1	1	1	1
2A	Multi Function Select 2 Register	1	0	0	0	1	1	1	1
2B	Multi Function Select 3 Register	0	0	0	0	1	1	1	1
2C	Multi Function Select 4 Register	1	0	0	0	1	1	1	1
2D	Wakeup Control Register	0	-	-	0	1	0	0	0

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Table 22 UART1 Device Configuration Registers

UART1 Device Configuration Registers (LDN CR01)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F2	Clock Source Select Register	-	-	-	-	-	-	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Select Register	0	0	0	0	0	-	0	0
FF	9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

Table 23 UART2 Device Configuration Registers

UART2 Device Configuration Registers (LDN CR02)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	IRQ Share Register	0	0	0	0	-	-	0	0
F1	IR Mode Select Register	-	-	-	0	0	1	0	0
F2	Clock Source Select Register	-	-	-	-	-	-	0	0
F4	9-bit Mode Slave Address Register	0	0	0	0	0	0	0	0
F5	9-bit Mode Slave Address Mask Register	0	0	0	0	0	0	0	0
F6	FIFO Select Register	0	0	0	0	0	-	0	0
FF	9-bit Mode Broadcast Address Register	1	1	1	1	1	1	1	1

Table 24 Parallel Port Device Configuration Registers

Parallel Port Device Configuration Registers (LDN CR03)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	0	1	0	0	0	0	1	0

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Table 25 Hardware Monitor Device Configuration Registers

Hardware Monitor Device Configuration Registers (LDN CR04)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

Table 26 KBC Device Configuration Registers

KBC Device Configuration Registers (LDN CR05)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
FE	PS/2 Swap Register	-	0	-	0	-	-	-	-

Table 27 GPIO Device Configuration Registers

GPIO Device Configuration Registers (LDN CR06)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	GPIO Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
70	GPIRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	GPIO0 Output Enable Register	-	0	0	0	0	0	0	0
F1	GPIO0 Output Data Register	1	1	1	1	1	1	1	1
F2	GPIO0 Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO0 Drive Enable Register	0	0	0	0	0	0	0	0
F4	GPIO0 SMI Enable Register	0	0	0	0	0	0	0	0
F5	GPIO0 SMI Detect Select Register	1	1	1	1	1	1	1	1
F6	GPIO0 SMI Status Register	0	0	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	1	1	1	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	0	0	0	0	0	0	0	0
E4	GPIO1 SMI Enable Register	0	0	0	0	0	0	0	0
E5	GPIO1 SMI Detect Select Register	1	1	1	1	1	1	1	1
E6	GPIO1 SMI Status Register	0	0	0	0	0	0	0	0

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D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	1	1	1	1	1	1	1	1
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register								
C4	GPIO3 SMI Enable Register	0	0	0	0	0	0	0	0
C5	GPIO3 SMI Detect Select Register	1	1	1	1	1	1	1	1
C6	GPIO3 SMI Status Register	0	0	0	0	0	0	0	0
B0	GPIO4 Output Enable Register	0	0	0	0	0	0	0	0
B1	GPIO4 Output Data Register	1	1	1	1	1	1	1	1
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
B3	GPIO4 Drive Enable Register	0	0	0	0	0	0	0	0
B4	GPIO4 SMI Enable Register	-	-	-	-	0	0	0	0
B5	GPIO4 SMI Detect Select Register	-	-	-	-	0	0	0	0
B6	GPIO4 SMI Status Register	-	-	-	-	0	0	0	0
A0	GPIO5 Output Enable Register	-	-	-	0	0	0	0	0
A1	GPIO5 Output Data Register	-	-	-	1	1	1	1	1
A2	GPIO5 Pin Status Register	-	-	-	-	-	-	-	-
A3	GPIO5 Drive Enable Register								
A4	GPIO5 SMI Enable Register	-	-	-	0	0	0	0	0
A5	GPIO5 SMI Detect Select Register	-	-	-	1	1	1	1	1
A6	GPIO5 SMI Status Register	-	-	-	0	0	0	0	0
90	GPIO6 Output Enable Register	0	0	0	0	0	0	0	0
91	GPIO6 Output Data Register	1	1	1	1	1	1	1	1
92	GPIO6 Pin Status Register	-	-	-	-	-	-	-	-
93	GPIO6 Drive Enable Register	0	0	0	0	0	0	0	0
94	GPIO6 SMI Enable Register	-	-	-	-	0	0	0	0
95	GPIO6 SMI Detect Select Register	-	-	-	-	0	0	0	0
96	GPIO6 SMI Status Register	-	-	-	-	0	0	0	0
97	Scan Code Control Register 1	0	0	0	0	0	0	0	0
98	Scan Code Control Register 2	0	0	0	0	0	0	0	0
99	Scan Code Enable Register	1	1	1	1	1	1	1	1
9A	Break Code Enable Register	1	1	1	1	1	1	1	1
9B	Prefix Code Enable Register	1	1	1	1	1	1	1	1
9C	Make Code Register 0~7 (SCAN_BANK_SEL = 0~7)	0	0	0	0	0	0	0	0
9D	Prefix Code Register 0~7 (SCAN_BANK_SEL = 0~7)	1	1	1	0	0	0	0	0
9E	Make Code Status Register	0	0	0	0	0	0	0	0
9F	Break Code Status Register	0	0	0	0	0	0	0	0
80	GPIO7 Output Enable Register	0	0	0	0	0	0	0	0

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81	GPIO7 Output Data Register	1	1	1	1	1	1	1	1
82	GPIO7 Pin Status Register	-	-	-	-	-	-	-	-
83	GPIO7 Drive Enable Register	0	0	0	0	0	0	0	0

Table 28 WDT Device Configuration Registers

WDT Device Configuration Registers (LDN CR07)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	Watchdog device Base Address Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	Watchdog Output Enable Register	0	-	-	-	-	-	-	-
F5	Watchdog Control Configuration Register 1	0	0	0	1	0	0	1	0
F6	Watchdog Timer Configuration Register 2	0	1	0	1	0	0	0	0
F7	Watchdog PME Enable Configuration Register 2	-	0	0	-	-	-	-	0

Table 29 PME, ACPI, and ERP Power Saving Device Configuration Registers

PME, ACPI, and ERP Power Saving Device Configuration Registers (LDN CR0A)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	PME Device Enable Register	-	-	-	-	-	-	-	0
E0	ERP Enable Register	0	0	0	0	0	0	0	0
E1	ERP Control Register 1	1	1	0	0	1	1	0	0
E2	ERP Control Register 2	1	0	0	0	0	0	0	0
E3	ERP PSIN De-bounce Register	0	0	0	1	0	0	1	1
E4	ERP RSMRST De-bounce Register	0	0	0	0	1	0	0	1
E5	ERP PSOUT De-bounce Register	1	1	0	0	0	1	1	1
E6	ERP PS_ON De-bounce Register	0	0	0	0	1	0	0	1
E7	ERP Deep S5 Delay Register	0	1	1	0	0	0	1	1
E8	ERP Wakeup Enable Register	0	0	0	1	0	0	0	0
E9	ERP Deep S3 Delay Register	0	0	0	0	1	1	1	1
EC	ERP Mode Select Register	0	0	-	-	-	-	-	-
ED	ERP WDT Control Register	0	0	-	-	0	0	0	0
EE	ERP WDT Timer	0	0	0	0	0	0	0	0
F0	PME Event Enable 1 Register	0	0	0	0	0	0	0	-
F1	PME Event Status 1 Register	-	-	-	-	-	-	-	-
F2	PME Event Enable 2 Register	-	-	-	-	-	0	0	0
F3	PME Event Status 2 Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register 1	0	0	0	0	0	1	1	1
F5	ACPI Control Register 2	1	0	0	0	1	-	0	0
F6	ACPI Control Register 3	0	0	0	1	1	1	1	1
F7	ACPI Control Register 4	1	0	0	0	0	1	1	0

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F8	LED VCC Control Register	0	0	0	0	0	0	0	0
F9	LED VSB Control Register	0	0	0	0	0	0	0	0
FA	LED Additional Control Register	0	0	0	0	0	0	0	0
FB	ACPI Control Register 5	0	0	0	0	0	0	0	0
FC	ACPI Control Register 6	0	0	0	0	0	1	1	1
FE	RI De-bounce Select Register	-	-	-	-	-	-	0	0

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5.2 Global Control Registers

5.2.1 Software Reset Register — Index 02h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	SOFT_RST	W	-	-	Write 1 to reset the register and device powered by VDD (3VCC).

5.2.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-0	LDN	R/W	LRESET#	00h	01h: Select UART1 device configuration registers. 02h: Select UART2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select WDT device configuration registers. 0Ah: Select PME, ACPI and ERP device configuration registers. Otherwise: Reserved.

5.2.3 Chip ID Register 1 — Index 20h

Bit	Name	R/W	Default	Description
7-0	Chip_ID1	R	12h	Chip ID1

5.2.4 Chip ID Register 2 — Index 21h

Bit	Name	R/W	Default	Description
7-0	Chip_ID2	R	10h	Chip ID2

5.2.5 Vendor ID Register 1 — Index 23h

Bit	Name	R/W	Default	Description
7-0	Vendor_ID1	R	19h	Vendor ID1

5.2.6 Vendor ID Register 2 — Index 24h

Bit	Name	R/W	Default	Description
7-0	Vendor_ID2	R	34h	Vendor ID2

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5.2.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	SOFTPD_PRT	R/W	3VCC	0	Write “1” to power down parallel port.
2	SOFTPD_UR2	R/W	3VCC	0	Write “1” to power down UART 2.
1	SOFTPD_UR1	R/W	3VCC	0	Write “1” to power down UART 1.
0	Reserved	-	-	-	Reserved.

5.2.8 Clock Select Register — Index 26h

Bit	Name	R/W	Reset	Default	Description
7	CLK_SEL	R/W	3VCC	0	The clock source of CLKIN. 0: CLKIN is 48MHz 1: CLKIN is 24MHz
6	Reserved	-	-	-	Reserved
5	DPORT_DEC_SEL	R/W	3VCC	0	Select the debug port address. 0: 0x80. 1: UART2 base address + 7. (UART 2 need to be enabled)
4	Reserved	-	-	-	Reserved
3	FUNC_PROG_SEL	R/W	3VCC	0	Index 0x29, 0x2B and 0x2C bank select register.
2-0	Reserved	R/W	3VCC	0	Dummy registers.

5.2.9 Configuration Port Select Register — Index 27h

Bit	Name	R/W	Reset	Default	Description
7	OVP_MODE	R/W	VBAT	1	OVP/UVP mode select. 0: OVP/UVP is auto enabled after power on. 1: OVP/UVP is enabled by registers.
6	TEMP_OUT_EN	R/W	LRESET#	0	Set this bit to “1” will output the CPU temperature to the 7-segment LED.
5	DPORT_EN	R/W	3VCC	0	0: The 80 port function is disabled. 1: The 80 port function is enabled.
4	PORT_4E_EN	R/W	3VCC	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1/ STRAP4E_2E. Pull down to select port 2E/2F.
3	GPIO5_RST_SEL	R/W	VBAT	0	0: GPIO5 registers are reset by 3VA. 1: GPIO5 registers are reset by VBAT.
2	GPIO3_RST_SEL	R/W	VBAT	0	0: GPIO3 registers are reset by 3VA. 1: GPIO3 registers are reset by VBAT.

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1	AT_ATX_MODE	R/W	VBAT	0	0: ATX mode. 1: AT mode. This register is power on trapped by AT_ATX_STRAP when 3VA power on.
0	TIMING_EN	R/W	VBAT	0	0: Disable power sequence (Intel Mode). 1: Enable power sequence (AMD Mode). This register is power on trapped by AT_ATX_STRAP when 3VA power on.

5.2.10 TSI Level Select Register — Index 28h (FUNC_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7	S3_GATE_EN	R/W	VBAT	1	0: Pin 56 functions as GPIO05/WDTRST#. 1: Pin 56 functions as S3_GATE#.
6	GPIO06_EN	R/W	VBAT	1	0: Pin 57 functions as SCL. 1: Pin 57 functions as GPIO06.
5	GPIO05_EN	R/W	VBAT	1	This would be affected only if S3_GATE_EN is not set. 0: Pin 56 functions as WDTRST#. 1: Pin 56 functions as GPIO05.
4	GPIO04_EN	R/W	VBAT	0	This would be affected only if S3P5_GATE_EN is not set. 0: Pin 55 functions as SLOTOCC#. 1: Pin 55 functions as GPIO04.
3	TSI3_LVL_SEL	R/W	VBAT	0	Select MCLK/MDATA input level. 0: TTL level. 1: Low input level.
2	TSI2_LVL_SEL	R/W	VBAT	0	Select GPIO02/GPIO03 input level. 0: TTL level. 1: Low input level.
1	TSI1_LVL_SEL	R/W	VBAT	0	Select GPIO00/GPIO01 input level. 0: TTL level. 1: Low input level.
0	TSI0_LVL_SEL	R/W	VBAT	0	Select GPIO06 input level. 0: TTL level. 1: Low input level.

5.2.11 TSI Pin Select Register — Index 28h (FUNC_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	PWRON_4S_Delay	R/W	VBAT	0	0: Disable delay 4 sec function. 1: Enable delay 4 sec function When power on S3# delay 4 sec after AC resume.
6	Reserved	R/W	VBAT	0	Dummy registers.

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5-4	TSI_PIN_SEL	R/W	VBAT	00	Select pins for TSI protocol. 00: Via pin 57 (GPIO06) / 58 (PECI) if enabled. 01: Via pin 49 (GPIO00) / 50 (GPIO01) if enabled. 10: Via pin 51 (GPIO02) / 52 (GPIO03) if enabled. 11: Via pin 71 (MDATA) / 72 (MCLK) if enabled.
3-2	MXM_PIN_SEL	R/W	VBAT	00	Select pins for MXM protocol. 00: Via pin 57 (GPIO06) / 58 (PECI) if enabled. 01: Via pin 49 (GPIO00) / 50 (GPIO01) if enabled. 10: Via pin 51 (GPIO02) / 52 (GPIO03) if enabled. 11: Via pin 71 (MDATA) / 72 (MCLK) if enabled.
1-0	I2C_PIN_SEL	R/W	VBAT	00	Select pins for I2C slave. 00: Via pin 57 (GPIO06) / 58 (PECI) if enabled. 01: Via pin 49 (GPIO00) / 50 (GPIO01) if enabled. 10: Via pin 51 (GPIO02) / 52 (GPIO03) if enabled. 11: Via pin 71 (MDATA) / 72 (MCLK) if enabled.

5.2.12 Multi Function Select 1 Register — Index 29h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_EN	R/W	VBAT	0	0: Pin 66 functions as CPU_PWRGD. 1: Pin 66 functions as GPIO17.
6	GPIO16_EN	R/W	VBAT	1	This bit only has effect if OVT_PIN_EN is not set. 0: Pin 65 functions as LED_VCC. 1: Pin 65 functions as GPIO16.
5	GPIO15_EN	R/W	VBAT	1	This bit only has effect if LED_VSB_EN is not set. 0: Pin 64 functions as ALERT#. 1: Pin 64 functions as GPIO15.
4	GPIO14_EN	R/W	VBAT	0	0: Pin 63 functions as WDTRST#. 1: Pin 63 functions as GPIO14.
3	GPIO13_EN	R/W	VBAT	1	This bit only has effect if S0P5_GATE_EN is not set. 0: Pin 62 functions as BEEP. 1: Pin 62 functions as GPIO13.
2	GPIO12_EN	R/W	VBAT	1	0: Pin 61 functions as RSTCON#. 1: Pin 61 functions as GPIO12.
1	GPIO11_EN	R/W	VBAT	1	0: Pin 60 functions as PCI_RST5#. 1: Pin 60 functions as GPIO11.
0	GPIO10_EN	R/W	VBAT	1	0: Pin 59 functions as PCI_RST4#. 1: Pin 59 functions as GPIO10.

5.2.13 Multi Function Select 2 Register — Index 2Ah

Bit	Name	R/W	Reset	Default	Description

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7	LPT_GP_EN	R/W	VBAT	1	LPT, GPIO6 and GPIO7 multi-function select. (Exclude pin 104). 0: Pin 100 ~ 116 functions as LPT. 1: Pin 100 ~ 116 functions as GPIO6X and GPIO7X.
6	GP_WDT_RST_EN	R/W	VBAT	0	Set “1” to reset GPIO45_EN/GPIO46_EN when WDT timeout occurs.
5	LED_VSB_EN	R/W	VBAT	0	0: Pin 64 functions as GPIO15/ALERT#. 1: Pin 64 functions as LED_VSB.
4	OVT_PIN_FUNC_SEL	R/W	VBAT	0	0: Pin 67 functions as OVT#. 1: Pin 67 functions as GPIO16/LED_VCC.
3	S0P5_GATE_EN	R/W	VBAT	1	0: Pin 62 functions as GPIO13/BEEP. 1: Pin 62 functions as S0P5_GATE#.
2	S3P5_GATE_EN	R/W	VBAT	1	0: Pin 55 functions as SLOTOCC#/GPIO04. 1: Pin 55 functions as S3P5_GATE#.
1-0	UR2_GP_SEL	R/W	VBAT	11b	UART2 and GPIO2 multi-function select. This bit would be only effect if DPORT_EN is not set. When DPORT_EN is set, UART2 pins function as 7 segment LED control pins to display debug port value. 00: Full UART2. All pins are used for UART2. 01: Simple UART2. Only SIN2 and SOUT2 are used. 10: Modem control. RTS2#, RI2#, DSR2#, DCD2#, CTS2# and DTR2# are used. 11: Function as GPIO2.

5.2.14 Multi Function Select 3 Register — Index 2Bh

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_EN	R/W	3VA	0	0: Pin 83 functions as PS_ON#. 1: Pin 83 functions as GPIO47.
6	GPIO46_EN	R/W	3VA	0	0: Pin 81 functions as PSOUT#. 1: Pin 81 functions as GPIO46. This bit could be reset by WDT timeout.
5	GPIO45_EN	R/W	3VA	0	0: Pin 80 functions as PSIN#. 1: Pin 80 functions as GPIO45. This bit could be reset by WDT timeout.
4	GPIO44_EN	R/W	3VA	0	0: Pin 84 functions as PWROK. 1: Pin 84 functions as GPIO44.
3	GPIO43_EN	R/W	3VA	1	0: Pin 28 functions as IRRX. 1: Pin 28 functions as GPIO43.
2	GPIO42_EN	R/W	3VA	1	0: Pin 27 functions as IRTX. 1: Pin 27 functions as GPIO42.
1	GPIO41_EN	R/W	3VA	1	0: Pin 26 functions as FANCTRL3. 1: Pin 26 functions as GPIO41.

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0	GPIO40_EN	R/W	3VA	1	0: Pin 25 functions as FANIN3. 1: Pin 25 functions as GPIO40.

5.2.15 Multi Function Select 4 Register — Index 2Ch

Bit	Name	R/W	Reset	Default	Description
7	MS_PIN_EN	R/W	VBAT	1	0: Pin 71/72 function as SDA/SCL. 1: Pin 71/72 function as MDATA/MCLK.
6	GPIO0_RST_SEL	R/W	VBAT	0	0: GPIO0 registers are reset by 3VA. 1: GPIO0 registers are reset by VBAT.
5	SDA_PIN58_EN	R/W	VBAT	0	0: Pin 58 functions as PECI. 1: Pin 58 functions as SDA.
4	VCORE_RST_DIS	R/W	VBAT	0	0: VLDT_EN and CPU_PWRGD will force low when VCORE browns out. 1: VLDT_EN and CPU_PWRGD remain un-affected when VCORE browns out.
3	GPIO03_EN	R/W	VBAT	1	0: Pin 52 functions as SDA. 1: Pin 52 functions as GPIO03.
2	GPIO02_EN	R/W	VBAT	1	0: Pin 51 functions as SCL. 1: Pin 51 functions as GPIO02.
1	GPIO01_EN	R/W	VBAT	1	0: Pin 50 functions as SDA. 1: Pin 50 functions as GPIO01.
0	GPIO00_EN	R/W	VBAT	1	0: Pin 49 functions as SCL. 1: Pin 49 functions as GPIO00.

5.2.16 Wakeup Control Register — Index 2Dh

Bit	Name	R/W	Reset	Default	Description
7	SLOTOCC_PWR_SEL	R/W	VBAT	0	SLOTOCC# power select. 0: SLOTOCC# is pull up to 3VSB. 1: SLOTOCC# is pull up to VBAT.
6-5	Reserved	-	-	-	Reserved
4	KEY_SEL_ADD	R/W	VBAT	0	Refer to KEY_SEL.
3	WAKEUP_EN	R/W	VBAT	1	0: disable KB/Mouse wakeup function. 1: enable KB/Mouse wakeup function.

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<table>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>VBAT</td><td>00</td><td>Select the keyboard wakeup key. Accompany with KEY_SEL_ADD, there are several key select as below:
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wakeup Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + Space</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup Key</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power Key</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + Space</td></tr>
<tr><td>1</td><td>11</td><td>Space</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>VBAT</td><td>0</td><td>Select the mouse wakeup key.
0: Wakeup by mouse clicking.
1: Wakeup by mouse clicking or movement.</td></tr>
</table>

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5.3 UART1 Registers (LDN 0x01)

5.3.1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UR1_EN	R/W	LRESET#	1	0: disable UART 1 I/O Port. 1: enable UART 1 I/O Port.

5.3.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of UART 1 base address.

5.3.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	F8h	The LSB of UART 1 base address.

5.3.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR1IRQ	R/W	LRESET#	4h	Select the IRQ channel for UART 1.

5.3.5 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	9BIT_MODE	R/W	LRESET#	0	0: normal UART function 1: enable 9-bit mode (multi-drop mode). In the 9-bit mode, the parity bit becomes the address/data bit.
6	AUTO_ADDR	R/W	LRESET#	0	This bit works only at 9-bit mode. 0: the SM2 bit will be cleared by host, so that data could be received. 1: the SM2 bit will be cleared by hardware according to the sent address and the given address (or broadcast address derived by SADDR and SADEN)
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise it is keeping low.

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3-2	Reserved	-	-	-	Reserved.
1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART1 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

5.3.6 Clock Source Select Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UR1_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART1. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.3.7 9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address at the 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 1. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 2. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Broadcast address could be programmed by BADDR register, if BADDR is programmed broadcast address calculated by SADDR is ignored. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

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5.3.8 9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 3. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 4. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Ex. SADDR: 0101_1100b SADEN: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

5.3.9 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LREST#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LREST#	0	IRQ_MODE1 and IRQ_MODE0 (UART1 IRQ Share Register — Index F0h, bit1) will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART1 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

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5.3.10 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

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5.4 UART2 Registers (LDN 0x02)

5.4.1 Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	UR2_EN	R/W	LRESET#	0	0: disable UART 2 I/O Port. 1: enable UART 2 I/O Port.

5.4.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	02h	The MSB of UART 2 base address.

5.4.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET	F8h	The LSB of UART 2 base address.

5.4.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELUR2IRQ	R/W	LRESET#	3h	Select the IRQ channel for UART 2.

5.4.5 IRQ Share Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	-	Reserved.
5	RS485_INV	R/W	LRESET#	0	Invert RTS# if RS485_EN is set.
4	RS485_EN	R/W	LRESET#	0	0: RS232 driver. 1: RS485 driver. RTS# is driven high automatically when transmitting data, otherwise it's keeping low.
3	RXW4C_IR	R/W	LRESET#	0	0 : No reception delay when SIR is changed from TX to RX. 1 : Reception delay 4 character-time when SIR is changed from TX to RX.
2	TXW4C_IR	R/W	LRESET#	0	0 : No transmission delay when SIR is changed from RX to TX. 1 : Transmission delay 4 character-time when SIR is changed from RX to TX.

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1	IRQ_MODE0	R/W	LRESET#	0	IRQ_MODE1 (UART2 FIFO Select Register — Index F6h, bit3) and IRQ_MODE0 will select the UART2 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE, bit 1).
0	IRQ_SHARE	R/W	LRESET#	0	0 : IRQ is not sharing with the other device. 1 : IRQ is sharing with the other device.

5.4.6 Clock Source Select Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	-	Reserved.
1-0	UR2_CLK_SEL	R/W	LRESET#	0	Select the clock source for UART2. 00: 1.8432MHz. 01: 18.432MHz. 10: 24MHz. 11: 14.769MHz.

5.4.7 9-bit Mode Slave Address Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7-0	SADDR	R/W	LRESET#	00h	This byte accompanying with SADEN will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 5. given address: If bit n of SADEN is “0”, then the corresponding bit of SADDR is don’t care. 6. broadcast address: If bit n of ORed SADDR and SADEN is “0”, don’t care that bit. The remaining bit which is “1” is compared to the received address. Broadcast address could be programmed by BADDR register, if BADDR is programmed, broadcast address calculated by SADDR is ignored. Ex.

SADDR	0101_1100b
SADEN	1111_1001b
Given Address	0101_1xx0b
Broadcast Address	1111_11x1b

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5.4.8 9-bit Mode Slave Address Mask Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-0	SADEN	R/W	LRESET#	00h	This byte accompanying with SADDR will determine the given address and broadcast address in 9-bit mode. The UART will response to both given and broadcast address. Following description determines the given address and broadcast address: 7. given address: If bit n of SADEN is "0", then the corresponding bit of SADDR is don't care. 8. broadcast address: If bit n of ORed SADDR and SADEN is "0", don't care that bit. The remaining bit which is "1" is compared to the received address. Ex. SADDR: 0101_1100b SADEN: 1111_1001b Given Address: 0101_1xx0b Broadcast Address: 1111_11x1b

5.4.9 FIFO Select Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	TX_DEL_1BIT	R/W	LREST#	0	0: TX will start transmit immediately after writing THR. 1: TX will delay 1 bit time to transmit after writing THR.
6	TX_INT_MODE	R/W	LRESET#	0	0: TX will assert interrupt when THR is empty. 1: TX will assert interrupt when THR and shift register is empty.
5-4	RXFTHR_MODE	R/W	LRESET#	0	The RX FIFO threshold select. 00: FIFO threshold is set by RXFTHR. 01: FIFO threshold will be 2X of RXFTHR. 10: FIFO threshold will be 4X of RXFTHR. 11: FIFO threshold will be 8X of RXFTHR.
3	IRQ_MODE1	R/W	LREST#	0	IRQ_MODE1 and IRQ_MODE0 (UART1 IRQ Share Register — Index F0h, bit1) will select the UART1 interrupt mode if IRQ sharing is enabled. 00 : Sharing IRQ active low Level mode. 01 : Sharing IRQ active high edge mode. 10 : Sharing IRQ active high Level mode. 11 : Reserved. This bit is effective at IRQ is sharing with the other device (IRQ_SHARE= 1, UART1 IRQ share register— index F0h, bit 0).
2	Reserved	-	-	-	Reserved.
1-0	FIFO_MODE	R/W	LRESET#	00h	Select the FIFO depth. 00: 16-byte FIFO. 01: 32-byte FIFO. 10: 64-byte FIFO. 11: 128-byte FIFO.

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5.4.10 9-bit Mode Broadcast Address Register — Index FFh

Bit	Name	R/W	Reset	Default	Description
7-0	BADDR	R/W	LRESET#	FFh	Broadcast address for 9-bit mode. Write this byte to set broadcast address instead of the one calculated by SADDR.

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5.5 UART Register

5.5.1 Receiver Buffer Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	RBR	R	LRESET#	00h	The data received. Read only when LCR [7] is 0

5.5.2 Transmitter Holding Register — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	THR	W	LRESET#	00h	Data to be transmitted. Write only when LCR [7] is 0

5.5.3 Divisor Latch (LSB) — Base + 0

Bit	Name	R/W	Reset	Default	Description
7-0	DLL	R/W	LRESET#	01h	Baud generator divisor low byte. Access only when LCR [7] is 1.

5.5.4 Divisor Latch (MSB) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-0	DLM	R/W	LRESET#	00h	Baud generator divisor high byte. Access only when LCR [7] is 1.

5.5.5 Interrupt Enable Register (IER) — Base + 1

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	SM2	R/WC	LRESET#	0	This bit is used only in 9-bit mode and always returns “0” when 9-bit mode is disabled. 0: The receiver could receive data byte. 1: The receiver could only receive address byte and issue an interrupt when the address is received.
3	EDSSI	R/W	LRESET#	0	Enable Modem Status Interrupt. Access only when LCR [7] is 0.
2	ELSI	R/W	LRESET#	0	Enable Line Status Error Interrupt. Access only when LCR [7] is 0.
1	ETBFI	R/W	LRESET#	0	Enable Transmitter Holding Register Empty Interrupt. Access only when LCR [7] is 0.
0	ERBFI	R/W	LRESET#	0	Enable Received Data Available Interrupt. Access only when LCR [7] is 0.

5.5.6 Interrupt Identification Register (IIR) — Base + 2

Bit	Name	R/W	Reset	Default	Description

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7	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
6	FIFO_EN	R	LRESET#	0	0: FIFO is disabled 1: FIFO is enabled.
5-4	Reserved	-	LRESET#	-	Reserved.
3-1	IRQ_ID	R	LRESET#	00	000: Interrupt is caused by Modem Status 001: Interrupt is caused by Transmitter Holding Register Empty 010: Interrupt is caused by Received Data Available. 110: Interrupt is caused by Character Timeout 011: Interrupt is caused by Line Status.
0	IRQ_PENDN	R	LRESET#	1	1: Interrupt is not pending. 0: Interrupt is pending.

5.5.7 FIFO Control Register — Base + 2

Bit	Name	R/W	Reset	Default	Description
7-6	RCV_TRIG	W	LRESET#	00	00: Receiver FIFO trigger level is 1. 01: Receiver FIFO trigger level is 4. 10: Receiver FIFO trigger level is 8. 11: Receiver FIFO trigger level is 14.
5-3	Reserved	-	LRESET#	-	Reserved.
2	CLRTX	R	LRESET#	0	Reset the transmitter FIFO.
1	CLRRX	R	LRESET#	0	Reset the receiver FIFO.
0	FIFO_EN	R	LRESET#	0	0: Disable FIFO. 1: Enable FIFO.

5.5.8 Line Control Register (LCR) — Base + 3

Bit	Name	R/W	Reset	Default	Description
7	DLAB	R/W	LRESET#	0	0: Divisor Latch can't be accessed. 1: Divisor Latch can be accessed via Base and Base+1.
6	SETBRK	R/W	LRESET#	0	0: Transmitter is in normal condition. 1: Transmit a break condition.
5	STKPAR	R/W	LRESET#	0	XX0: Parity Bit is disable 001: Parity Bit is odd. 011: Parity Bit is even 101: Parity Bit is logic 1 111: Parity Bit is logic 0
4	EPS	R/W	LRESET#	0	
3	PEN	R/W	LRESET#	0	
2	STB	R/W	LRESET#	0	0: Stop bit is one bit 1: When word length is 5 bit stop bit is 1.5 bit else stop bit is 2 bit
1-0	WLS	R/W	LRESET#	00	00: Word length is 5 bit 01: Word length is 6 bit 10: Word length is 7 bit 11: Word length is 8 bit

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5.5.9 MODEM Control Register (MCR) — Base + 4

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	LRESET#	-	Reserved.
4	LOOP	R/W	LRESET#	0	0: UART in normal condition. 1: UART is internal loop back
3	OUT2	R/W	LRESET#	0	0: All interrupt is disabled. 1: Interrupt is enabled (disabled) by IER.
2	OUT1	R/W	LRESET#	0	Read from MSR[6] while in loop back mode
1	RTS	R/W	LRESET#	0	0: RTS# is forced to logic 1 1: RTS# is forced to logic 0
0	DTR	R/W	LRESET#	0	0: DTR# is forced to logic 1 1: DTR# is forced to logic 0

5.5.10 Line Status Register (LSR) — Base + 5

Bit	Name	R/W	Reset	Default	Description
7	RCR_ERR	R	LRESET#	0	0: No error in the FIFO when FIFO is enabled 1: Error in the FIFO when FIFO is enabled.
6	TEMT	R	LRESET#	1	0: Transmitter is in transmitting. 1: Transmitter is empty.
5	THRE	R	LRESET#	1	0: Transmitter Holding Register is not empty. 1: Transmitter Holding Register is empty.
4	BI	R	LRESET#	0	0: No break condition detected. 1: A break condition is detected.
3	FE	R	LRESET#	0	0: Data received has no frame error. 1: Data received has frame error.
2	PE	R	LRESET#	0	0: Data received has no parity error. 1: Data received has parity error.
1	OE	R	LRESET#	0	0: No overrun condition occurred. 1: An overrun condition occurred.
0	DR	R	LRESET#	0	0: No data is ready for read. 1: Data is received.

5.5.11 MODEM Status Register (MSR) — Base + 6

Bit	Name	R/W	Reset	Default	Description
7	DCD	R	-	-	Complement of DCD# input. In loop back mode, this bit is equivalent to OUT2 in MCR.
6	RI	R	-	-	Complement of RI# input. In loop back mode , this bit is equivalent to OUT1 in MCR
5	DSR	R	-	-	Complement of DSR# input. In loop back mode , this bit is equivalent to DTR in MCR
4	CTS	R	-	-	Complement of CTS# input. In loop back mode , this bit is equivalent to RTS in MCR

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3	DDCD	R	LRESET#	0	0: No state changed at DCD#. 1: State changed at DCD#.
2	TERI	R	LRESET#	0	0: No Trailing edge at RI#. 1: A low to high transition at RI#.
1	DDSR	R	LRESET#	1	0: No state changed at DSR#. 1: State changed at DSR#.
0	DCTS	R	LRESET#	1	0: No state changed at CTS#. 1: State changed at CTS#.

5.5.12 Scratch Register — Base + 7

Bit	Name	R/W	Reset	Default	Description
7-0	SCR	R/W	LRESET#	00h	Scratch register.

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5.6 Parallel Port Register (CR03)

5.6.1 Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PRT_EN	R/W	LRESET#	0	0: disable Parallel Port. 1: enable Parallel Port.

5.6.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	03h	The MSB of Parallel Port base address.

5.6.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	78h	The LSB of Parallel Port base address.

5.6.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELPRTIRQ	R/W	LRESET#	7h	Select the IRQ channel for Parallel Port.

5.6.5 DMA Channel Select Register — Index 74h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved.
4	ECP_DMA_MODE	R/W	LRESET#	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	-	Reserved.
2-0	SELPRTDMA	R/W	LRESET#	011	Select the DMA channel for Parallel Port.

5.6.6 PRT Mode Select Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	SPP_IRQ_MODE	R/W	LRESET#	0	Interrupt mode in non-ECP mode. 0: Level mode. 1: Pulse mode.
6-3	ECP_FIFO_THR	R/W	LRESET#	1000	ECP FIFO threshold.

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2-0	PRT_MODE	R/W	LRESET#	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

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5.7 Hardware Monitor Registers (LDN 0x04)

5.7.1 Hardware Monitor Configuration Registers — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

5.7.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

5.7.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

5.7.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

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5.8 KBC Registers (LDN 0x05)

5.8.1 KBC Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	KBC_EN	R/W	3VCC	1	0: disable KBC. 1: enable KBC.

5.8.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of KBC command port address. The address of data port is command port address + 4

5.8.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

5.8.4 KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELKIRQ	R/W	LRESET#	1h	Select the IRQ channel for keyboard interrupt.

5.8.5 Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELMIRQ	R/W	LRESET#	Ch	Select the IRQ channel for PS/2 mouse interrupt.

5.8.6 PS/2 Swap Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	RE_GEN_INT_EN	R/W	VBAT	0	Set “1” to auto re-generate interrupt every 500ms if interrupt is not serviced.
5	Reserved	-	-	-	Reserved, Fintek Internal Used Registers Only.
4	KB_MO_SWAP	R/W	VBAT	0	Keyboard Mouse Swap. 0: Keyboard/Mouse is not swapped. 1: Keyboard/Mouse is swapped. This bit could be programmed by user.

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3-0	Reserved	-	-	-	Reserved, Fintek Internal Used Registers Only.

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5.9 GPIO Registers (LDN 0x06)

5.9.1 GPIO IO Port Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	GPIO_EN	R/W	LRESET#	1	0: disable GPIO. 1: enable GPIO.

5.9.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	0h	The MSB of GPIO base address.

5.9.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	0h	The LSB of GPIO base address.

5.9.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-0	SELGPIRQ	R/W	LRESET#	0h	Select the IRQ channel for GPIO.

5.9.5 GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_OE	R/W	LRESET#	-	0: GPIO07 is input. 1: GPIO07 is output.
6	GPIO06_OE	R/W	3VA/ VBAT	0	0: GPIO06 is input. 1: GPIO06 is output.
5	GPIO05_OE	R/W	3VA/ VBAT	0	0: GPIO05 is input. 1: GPIO05 is output.
4	GPIO04_OE	R/W	3VA/ VBAT	0	0: GPIO04 is input. 1: GPIO04 is output.
3	GPIO03_OE	R/W	3VA/ VBAT	0	0: GPIO03 is input. 1: GPIO03 is output.
2	GPIO02_OE	R/W	3VA/ VBAT	0	0: GPIO02 is input. 1: GPIO02 is output.
1	GPIO01_OE	R/W	3VA/ VBAT	0	0: GPIO01 is input. 1: GPIO01 is output.
0	GPIO00_OE	R/W	3VA/ VBAT	0	0: GPIO01 is input. 1: GPIO01 is output.

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5.9.6 GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_VAL	R/W	LRESET#	1	0: GPIO07 outputs 0 when in output mode. 1: GPIO07 outputs 1 when in output mode.
6	GPIO06_VAL	R/W	3VA/ VBAT	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs 1 when in output mode.
5	GPIO05_VAL	R/W	3VA/ VBAT	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	3VA/ VBAT	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	3VA/ VBAT	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	3VA/ VBAT	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	3VA/ VBAT	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO01_VAL	R/W	3VA/ VBAT	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.

5.9.7 GPIO0 Pin Status Register — Index F2h

Bit	Name	R/W	**Reset**	Default	Description
7	GPIO07_IN	R	-	-	The pin status of GPIO07.
6	GPIO06_IN	R	-	-	The pin status of GPIO06.
5	GPIO05_IN	R	-	-	The pin status of GPIO05.
4	GPIO04_IN	R	-	-	The pin status of GPIO04.
3	GPIO03_IN	R	-	-	The pin status of GPIO03.
2	GPIO02_IN	R	-	-	The pin status of GPIO02.
1	GPIO01_IN	R	-	-	The pin status of GPIO01.
0	GPIO01_IN	R	-	-	The pin status of GPIO01.

5.9.8 GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DRV_EN	R/w	LRESET#	0	0: GPIO07 is open drain. 1: GPIO07 is push pull.
6	GPIO06_DRV_EN	R/w	3VA/ VBAT	0	0: GPIO06 is open drain. 1: GPIO06 is push pull.
5	GPIO05_DRV_EN	R/w	3VA/ VBAT	0	0: GPIO05 is open drain. 1: GPIO05 is push pull.
4	Reserved	-	3VA/ VBAT	0	Dummy registers.

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3	GPIO03_DRV_EN	R/W	3VA/ VBAT	0	0: GPIO03 is open drain. 1: GPIO03 is push pull.
2	GPIO02_DRV_EN	R/W	3VA/ VBAT	0	0: GPIO02 is open drain. 1: GPIO02 is push pull.
1	GPIO01_DRV_EN	R/W	3VA/ VBAT	0	0: GPIO01 is open drain. 1: GPIO01 is push pull.
0	GPIO00_DRV_EN	R/W	3VA/ VBAT	0	0: GPIO00 is open drain. 1: GPIO00 is push pull.

5.9.9 GPIO0 SMI Enable Register — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO07_SMI_ST is set.
6	GPIO06_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO06_SMI_ST is set.
5	GPIO05_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO05_SMI_ST is set.
4	GPIO04_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO04_SMI_ST is set.
3	GPIO03_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO03_SMI_ST is set.
2	GPIO02_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO02_SMI_ST is set.
1	GPIO01_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO01_SMI_ST is set.
0	GPIO00_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO00_SMI_ST is set.

5.9.10 GPIO0 SMI Detect Select Register — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_DET_SEL	R/W	LRESET#	1	0: GPIO07 rising edge to set SMI status. 1: GPIO07 falling edge to set SMI status.
6	GPIO06_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO06 rising edge to set SMI status. 1: GPIO06 falling edge to set SMI status.
5	GPIO05_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO05 rising edge to set SMI status. 1: GPIO05 falling edge to set SMI status.
4	GPIO04_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO04 rising edge to set SMI status. 1: GPIO04 falling edge to set SMI status.
3	GPIO03_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO03 rising edge to set SMI status. 1: GPIO03 falling edge to set SMI status.
2	GPIO02_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO02 rising edge to set SMI status. 1: GPIO02 falling edge to set SMI status.

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1	GPIO01_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO01 rising edge to set SMI status. 1: GPIO01 falling edge to set SMI status.
0	GPIO00_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO00 rising edge to set SMI status. 1: GPIO00 falling edge to set SMI status.

5.9.11 GPIO0 SMI Status Register — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO07_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO07 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO06_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO06 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO05_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO05 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO04_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO04 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO03_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO03 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO02_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO02 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO01_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO01 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO00_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO00 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.9.12 GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_OE	R/W	3VA	0	0: GPIO17 is in input mode. 1: GPIO17 is in output mode.

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6	GPIO16_OE	R/W	3VA	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	3VA	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	3VA	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	3VA	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	3VA	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	3VA	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	3VA	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

5.9.13 GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_VAL	R/W	3VA	1	0: GPIO17 outputs 0 when in output mode. 1: GPIO17 outputs1 when in output mode.
6	GPIO16_VAL	R/W	3VA	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	3VA	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	3VA	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	3VA	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	3VA	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	3VA	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	3VA	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

5.9.14 GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_IN	R	-	-	The pin status of GPIO17.
6	GPIO16_IN	R	-	-	The pin status of GPIO16.
5	GPIO15_IN	R	-	-	The pin status of GPIO15.
4	GPIO14_IN	R	-	-	The pin status of GPIO14.
3	GPIO13_IN	R	-	-	The pin status of GPIO13.
2	GPIO12_IN	R	-	-	The pin status of GPIO12.

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1	GPIO11_IN	R	-	-	The pin status of GPIO11.
0	GPIO10_IN	R	-	-	The pin status of GPIO10.

5.9.15 GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DRV_EN	R/W	3VA	0	0: GPIO17 is open drain in output mode. 1: GPIO17 is push pull in output mode.
6	GPIO16_DRV_EN	R/W	3VA	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	3VA	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	3VA	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	3VA	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	3VA	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	3VA	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	3VA	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

5.9.16 GPIO1 SMI Enable Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO17_SMI_ST is set.
6	GPIO16_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO16_SMI_ST is set.
5	GPIO15_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO15_SMI_ST is set.
4	GPIO14_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO14_SMI_ST is set.
3	GPIO13_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO13_SMI_ST is set.
2	GPIO12_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO12_SMI_ST is set.
1	GPIO11_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO11_SMI_ST is set.
0	GPIO10_SMI_EN	R/W	3VA	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO10_SMI_ST is set.

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5.9.17 GPIO1 SMI Detect Select Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_DET_SEL	R/W	3VA	1	0: GPIO17 rising edge to set SMI status. 1: GPIO17 falling edge to set SMI status.
6	GPIO16_DET_SEL	R/W	3VA	1	0: GPIO16 rising edge to set SMI status. 1: GPIO16 falling edge to set SMI status.
5	GPIO15_DET_SEL	R/W	3VA	1	0: GPIO15 rising edge to set SMI status. 1: GPIO15 falling edge to set SMI status.
4	GPIO14_DET_SEL	R/W	3VA	1	0: GPIO14 rising edge to set SMI status. 1: GPIO14 falling edge to set SMI status.
3	GPIO13_DET_SEL	R/W	3VA	1	0: GPIO13 rising edge to set SMI status. 1: GPIO13 falling edge to set SMI status.
2	GPIO12_DET_SEL	R/W	3VA	1	0: GPIO12 rising edge to set SMI status. 1: GPIO12 falling edge to set SMI status.
1	GPIO11_DET_SEL	R/W	3VA	1	0: GPIO11 rising edge to set SMI status. 1: GPIO11 falling edge to set SMI status.
0	GPIO10_DET_SEL	R/W	3VA	1	0: GPIO10 rising edge to set SMI status. 1: GPIO10 falling edge to set SMI status.

5.9.18 GPIO1 SMI Status Register — Index E6h

Bit	Name	R/W	Reset	Default	Description
7	GPIO17_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO17 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO16_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO16 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO15_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO15 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO14_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO14 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO13_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO13 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

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2	GPIO12_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO12 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO11_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO11 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO10_SMI_ST	R/WC	3VA	0	0: No SMI event. 1: A SMI event will set if GPIO10 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.9.19 GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_OE	R/W	LRESET#	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	LRESET#	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	LRESET#	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4-0	Reserved	-	-	-	Reserved.

5.9.20 GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_VAL	R/W	LRESET#	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs1 when in output mode.
6	GPIO26_VAL	R/W	LRESET#	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs1 when in output mode.
5	GPIO25_VAL	R/W	LRESET#	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	LRESET#	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	LRESET#	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	LRESET#	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	LRESET#	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	LRESET#	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

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5.9.21 GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_IN	R	-	-	The pin status of GPIO27.
6	GPIO26_IN	R	-	-	The pin status of GPIO26.
5	GPIO25_IN	R	-	-	The pin status of GPIO25.
4	GPIO24_IN	R	-	-	The pin status of GPIO24.
3	GPIO23_IN	R	-	-	The pin status of GPIO23.
2	GPIO22_IN	R	-	-	The pin status of GPIO22.
1	GPIO21_IN	R	-	-	The pin status of GPIO21.
0	GPIO20_IN	R	-	-	The pin status of GPIO20.

5.9.22 GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO27_DRV_EN	R/W	LRESET#	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	LRESET#	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	LRESET#	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	LRESET#	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	LRESET#	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	LRESET#	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	LRESET#	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	LRESET#	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

5.9.23 GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_OE	R/W	3VA/ VBAT	0	0: GPIO37 is input. 1: GPIO37 is output.
6	GPIO36_OE	R/W	3VA/ VBAT	0	0: GPIO36 is input. 1: GPIO36 is output.
5	GPIO35_OE	R/W	3VA/ VBAT	0	0: GPIO35 is input. 1: GPIO35 is output.
4	GPIO34_OE	R/W	3VA/ VBAT	0	0: GPIO34 is input. 1: GPIO34 is output.

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3	GPIO33_OE	R/W	3VA/ VBAT	0	0: GPIO33 is input. 1: GPIO33 is output.
2	GPIO32_OE	R/W	3VA/ VBAT	0	0: GPIO32 is input. 1: GPIO32 is output.
1	GPIO31_OE	R/W	3VA/ VBAT	0	0: GPIO31 is input. 1: GPIO31 is output.
0	GPIO30_OE	R/W	3VA/ VBAT	0	0: GPIO30 is input. 1: GPIO30 is output.

5.9.24 GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_VAL	R/W	3VA/ VBAT	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.
6	GPIO36_VAL	R/W	3VA/ VBAT	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_VAL	R/W	3VA/ VBAT	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	3VA/ VBAT	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	3VA/ VBAT	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	3VA/ VBAT	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	3VA/ VBAT	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	3VA/ VBAT	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

5.9.25 GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_IN	R	-	-	The pin status of GPIO37.
6	GPIO36_IN	R	-	-	The pin status of GPIO36.
5	GPIO35_IN	R	-	-	The pin status of GPIO35.
4	GPIO34_IN	R	-	-	The pin status of GPIO34.
3	GPIO33_IN	R	-	-	The pin status of GPIO33.
2	GPIO32_IN	R	-	-	The pin status of GPIO32.
1	GPIO31_IN	R	-	-	The pin status of GPIO31.
0	GPIO30_IN	R	-	-	The pin status of GPIO30.

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5.9.26 GPIO3 SMI Enable Register — Index C4h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO37_SMI_ST is set.
6	GPIO36_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO36_SMI_ST is set.
5	GPIO35_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO35_SMI_ST is set.
4	GPIO34_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO34_SMI_ST is set.
3	GPIO33_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO33_SMI_ST is set.
2	GPIO32_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO32_SMI_ST is set.
1	GPIO31_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO31_SMI_ST is set.
0	GPIO30_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO30_SMI_ST is set.

5.9.27 GPIO3 SMI Detect Select Register — Index C5h

Bit	Name	R/W	Reset	Default	Description
7	GPIO37_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO37 rising edge to set SMI status. 1: GPIO37 falling edge to set SMI status.
6	GPIO36_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO36 rising edge to set SMI status. 1: GPIO36 falling edge to set SMI status.
5	GPIO35_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO35 rising edge to set SMI status. 1: GPIO35 falling edge to set SMI status.
4	GPIO34_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO34 rising edge to set SMI status. 1: GPIO34 falling edge to set SMI status.
3	GPIO33_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO33 rising edge to set SMI status. 1: GPIO33 falling edge to set SMI status.
2	GPIO32_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO32 rising edge to set SMI status. 1: GPIO32 falling edge to set SMI status.
1	GPIO31_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO31 rising edge to set SMI status. 1: GPIO31 falling edge to set SMI status.
0	GPIO30_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO30 rising edge to set SMI status. 1: GPIO30 falling edge to set SMI status.

5.9.28 GPIO3 SMI Status Register — Index C6h

Bit	Name	R/W	Reset	Default	Description

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7	GPIO37_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO37 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO36_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO36 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO35_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO35 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO34_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO34 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO33_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO33 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO32_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO32 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO31_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO31 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO30_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO30 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.9.29 GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_OE	R/W	3VA	0	0: GPIO47 is input. 1: GPIO47 is output.
6	GPIO46_OE	R/W	3VA	0	0: GPIO46 is input. 1: GPIO46 is output.
5	GPIO45_OE	R/W	3VA	0	0: GPIO45 is input. 1: GPIO45 is output.
4	GPIO44_OE	R/W	3VA	0	0: GPIO44 is input. 1: GPIO44 is output.
3	GPIO43_OE	R/W	LRESET#	0	0: GPIO43 is input. 1: GPIO43 is output.

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2	GPIO42_OE	R/W	LRESET#	0	0: GPIO42 is input. 1: GPIO42 is output.
1	GPIO41_OE	R/W	LRESET#	0	0: GPIO41 is input. 1: GPIO41 is output.
0	GPIO40_OE	R/W	LRESET#	0	0: GPIO40 is input. 1: GPIO40 is output.

5.9.30 GPIO4 Output Data Register — Index B1h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_VAL	R/W	3VA	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_VAL	R/W	3VA	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_VAL	R/W	3VA	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_VAL	R/W	3VA	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_VAL	R/W	LRESET#	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.
2	GPIO42_VAL	R/W	LRESET#	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_VAL	R/W	LRESET#	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_VAL	R/W	LRESET#	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

5.9.31 GPIO4 Pin Status Register — Index B2h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_ST	R	-	-	The pin status of GPIO47.
6	GPIO46_ST	R	-	-	The pin status of GPIO46.
5	GPIO45_ST	R	-	-	The pin status of GPIO45.
4	GPIO44_ST	R	-	-	The pin status of GPIO44.
3	GPIO43_ST	R	-	-	The pin status of GPIO43.
2	GPIO42_ST	R	-	-	The pin status of GPIO42.
1	GPIO41_ST	R	-	-	The pin status of GPIO41.
0	GPIO40_ST	R	-	-	The pin status of GPIO40.

5.9.32 GPIO4 Drive Enable Register — Index B3h

Bit	Name	R/W	Reset	Default	Description
7	GPIO47_DRV_EN	R/W	3VA	0	0: GPIO47 is open drain. 1: GPIO47 is push pull.

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6	GPIO46_DRV_EN	R/W	3VA	0	0: GPIO46 is open drain. 1: GPIO46 is push pull.
5	GPIO45_DRV_EN	R/w	3VA	0	0: GPIO45 is open drain. 1: GPIO45 is push pull.
4	GPIO44_DRV_EN	R/W	3VA	0	0: GPIO44 is open drain. 1: GPIO44 is push pull.
3	GPIO43_DRV_EN	R/W	LRESET#	0	0: GPIO43 is open drain. 1: GPIO43 is push pull.
2	GPIO42_DRV_EN	R/W	LRESET#	0	0: GPIO42 is open drain. 1: GPIO42 is push pull.
1	GPIO41_DRV_EN	R/W	LRESET#	0	0: GPIO41 is open drain. 1: GPIO41 is push pull.
0	GPIO40_DRV_EN	R/W	LRESET#	0	0: GPIO40 is open drain. 1: GPIO40 is push pull.

5.9.33 GPIO4 SMI Enable Register — Index B4h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	GPIO43_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO43_SMI_ST is set.
2	GPIO42_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO42_SMI_ST is set.
1	GPIO41_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO41_SMI_ST is set.
0	GPIO40_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO40_SMI_ST is set.

5.9.34 GPIO4 SMI Detect Select Register — Index B5h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	GPIO43_DET_SEL	R/W	LRESET#	1	0: GPIO43 rising edge to set SMI status. 1: GPIO43 falling edge to set SMI status.
2	GPIO42_DET_SEL	R/W	LRESET#	1	0: GPIO42 rising edge to set SMI status. 1: GPIO42 falling edge to set SMI status.
1	GPIO41_DET_SEL	R/W	LRESET#	1	0: GPIO41 rising edge to set SMI status. 1: GPIO41 falling edge to set SMI status.
0	GPIO40_DET_SEL	R/W	LRESET#	1	0: GPIO40 rising edge to set SMI status. 1: GPIO40 falling edge to set SMI status.

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5.9.35 GPIO4 SMI Status Register — Index B6h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved
3	GPIO43_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO43 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO42_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO42 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO41_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO41 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO40_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO40 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.9.36 GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO54_OE	R/W	3VA/ VBAT	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	3VA/ VBAT	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	3VA/ VBAT	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.
1	GPIO51_OE	R/W	3VA/ VBAT	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	3VA/ VBAT	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

5.9.37 GPIO5 Output Data Register — Index A1h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO54_VAL	R/W	3VA/ VBAT	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs 1 when in output mode.
3	GPIO53_VAL	R/W	3VA/ VBAT	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs 1 when in output mode.

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2	GPIO52_VAL	R/W	3VA/ VBAT	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs 1 when in output mode.
1	GPIO51_VAL	R/W	3VA/ VBAT	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs 1 when in output mode.
0	GPIO50_VAL	R/W	3VA/ VBAT	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs 1 when in output mode.

5.9.38 GPIO5 Pin Status Register — Index A2h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO54_ST	R	-	-	The pin status of GPIO54.
3	GPIO53_ST	R	-	-	The pin status of GPIO53.
2	GPIO52_ST	R	-	-	The pin status of GPIO52.
1	GPIO51_ST	R	-	-	The pin status of GPIO51.
0	GPIO50_ST	R	-	-	The pin status of GPIO50.

5.9.39 GPIO5 SMI Enable Register — Index A4h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO54_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO54_SMI_ST is set.
3	GPIO53_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO53_SMI_ST is set.
2	GPIO52_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO52_SMI_ST is set.
1	GPIO51_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO51_SMI_ST is set.
0	GPIO50_SMI_EN	R/W	3VA/ VBAT	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO50_SMI_ST is set.

5.9.40 GPIO5 SMI Detect Select Register — Index A5h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO54_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO54 rising edge to set SMI status. 1: GPIO54 falling edge to set SMI status.
3	GPIO53_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO53 rising edge to set SMI status. 1: GPIO53 falling edge to set SMI status.
2	GPIO52_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO52 rising edge to set SMI status. 1: GPIO52 falling edge to set SMI status.

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1	GPIO51_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO51 rising edge to set SMI status. 1: GPIO51 falling edge to set SMI status.
0	GPIO50_DET_SEL	R/W	3VA/ VBAT	1	0: GPIO50 rising edge to set SMI status. 1: GPIO50 falling edge to set SMI status.

5.9.41 GPIO5 SMI Status Register — Index A6h

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved
4	GPIO54_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO54 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO53_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO53 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO52_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO52 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO51_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO51 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO50_SMI_ST	R/WC	3VA/ VBAT	0	0: No SMI event. 1: A SMI event will set if GPIO50 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

5.9.42 GPIO6 Output Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_OE	R/W	LRESET#	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	LRESET#	0	0: GPIO66 is in input mode. 1: GPIO65 is in output mode.
5	GPIO65_OE	R/W	LRESET#	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	LRESET#	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	LRESET#	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.
2	GPIO62_OE	R/W	LRESET#	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.

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1	GPIO61_OE	R/W	LRESET#	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	LRESET#	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

5.9.43 GPIO6 Output Data Register — Index 91h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_VAL	R/W	LRESET#	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_VAL	R/W	LRESET#	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_VAL	R/W	LRESET#	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_VAL	R/W	LRESET#	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_VAL	R/W	LRESET#	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.
2	GPIO62_VAL	R/W	LRESET#	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.
1	GPIO61_VAL	R/W	LRESET#	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_VAL	R/W	LRESET#	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

5.9.44 GPIO6 Pin Status Register — Index 92h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_IN	R	-	-	The pin status of GPIO67.
6	GPIO66_IN	R	-	-	The pin status of GPIO66.
5	GPIO65_IN	R	-	-	The pin status of GPIO65.
4	GPIO64_IN	R	-	-	The pin status of GPIO64.
3	GPIO63_IN	R	-	-	The pin status of GPIO63.
2	GPIO62_IN	R	-	-	The pin status of GPIO62.
1	GPIO61_IN	R	-	-	The pin status of GPIO61.
0	GPIO60_IN	R	-	-	The pin status of GPIO60.

5.9.45 GPIO6 Drive Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_DRV_EN	R/W	LRESET#	0	0: GPIO67 is open drain in output mode. 1: Reserved.
6	GPIO66_DRV_EN	R/W	LRESET#	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.

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5	GPIO65_DRV_EN	R/W	LRESET#	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	LRESET#	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.
3	GPIO63_DRV_EN	R/W	LRESET#	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	LRESET#	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	LRESET#	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	LRESET#	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

5.9.46 GPIO6 SMI Enable Register — Index 94h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO67_SMI_ST is set.
6	GPIO66_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO66_SMI_ST is set.
5	GPIO65_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO65_SMI_ST is set.
4	GPIO64_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO64_SMI_ST is set.
3	GPIO63_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO63_SMI_ST is set.
2	GPIO62_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO62_SMI_ST is set.
1	GPIO61_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO61_SMI_ST is set.
0	GPIO60_SMI_EN	R/W	LRESET#	0	0: Disable SMI event. 1: Enable SMI event via PME# or SIRQ if GPIO60_SMI_ST is set.

5.9.47 GPIO6 SMI Detect Select Register — Index 95h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_DET_SEL	R/W	LRESET#	1	0: GPIO67 rising edge to set SMI status. 1: GPIO67 falling edge to set SMI status.
6	GPIO66_DET_SEL	R/W	LRESET#	1	0: GPIO66 rising edge to set SMI status. 1: GPIO66 falling edge to set SMI status.
5	GPIO65_DET_SEL	R/W	LRESET#	1	0: GPIO65 rising edge to set SMI status. 1: GPIO65 falling edge to set SMI status.
4	GPIO64_DET_SEL	R/W	LRESET#	1	0: GPIO64 rising edge to set SMI status. 1: GPIO64 falling edge to set SMI status.

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3	GPIO63_DET_SEL	R/W	LRESET#	1	0: GPIO63 rising edge to set SMI status. 1: GPIO63 falling edge to set SMI status.
2	GPIO62_DET_SEL	R/W	LRESET#	1	0: GPIO62 rising edge to set SMI status. 1: GPIO62 falling edge to set SMI status.
1	GPIO61_DET_SEL	R/W	LRESET#	1	0: GPIO61 rising edge to set SMI status. 1: GPIO61 falling edge to set SMI status.
0	GPIO60_DET_SEL	R/W	LRESET#	1	0: GPIO60 rising edge to set SMI status. 1: GPIO60 falling edge to set SMI status.

5.9.48 GPIO6 SMI Status Register — Index 96h

Bit	Name	R/W	Reset	Default	Description
7	GPIO67_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO67 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
6	GPIO66_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO66 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
5	GPIO65_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO65 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
4	GPIO64_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO64 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
3	GPIO63_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO63 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
2	GPIO62_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO62 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
1	GPIO61_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO61 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.
0	GPIO60_SMI_ST	R/WC	LRESET#	0	0: No SMI event. 1: A SMI event will set if GPIO60 input is changed. This bit is available in input mode. Write “1” to this bit will clear the status.

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5.9.49 Scan Code Control Register 1 — Index 97h

Bit	Name	R/W	Reset	Default	Description
7-6	REP_DEL_TIME	R/W	3VA	0	Delay time for repeating the make code. 00: 500 ~ 750ms. 01: 750 ~ 1000ms. 10: 1000 ~ 1250ms. 11: 1250 ~ 1500ms.
5-4	REP_TIME	R/W	3VA	0	Repeat time when the key is pressed. 00: 20 times per second. 01: 10 times per second. 10: 4 times per second. 11: 2 timers per second.
3	DIS_REP_EVENT	R/W	3VA	0	Disable repeating the make code when key is pressed.
2	Reserved	R/W	3VA	0	Dummy register.
1	PSEUDO_8048_EN	R/W	3VA	0	Set “1” to enable auto response to KBC command. It will return 0xFA, 0xAA for 0xFF command and 0xFA for other commands. This bit is used for GPIO scan code function without PS/2 keyboard.
0	GP_KB_EN	R/W	3VA	0	Set this bit to enable KeyBoard key emulation function.

5.9.50 Scan Code Control Register 2 — Index 98h

Bit	Name	R/W	Reset	Default	Description
7	CTRL_ALT_EN7	R/W	3VA	0	0: Make code/ break code are asserted when GPIO67 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
6	CTRL_ALT_EN6	R/W	3VA	0	0: Make code/ break code are asserted when GPIO66 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
5	CTRL_ALT_EN5	R/W	3VA	0	0: Make code/ break code are asserted when GPIO65 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
4	CTRL_ALT_EN4	R/W	3VA	0	0: Make code/ break code are asserted when GPIO64 is pressed /released. 1: Ctrl + Alt are asserted before make/break code.
3	Reserved	R/W	3VA	0	Reserved.
0	SCAN_BANK_SEL	R/W	3VA	0	Bank select to program pre-code and make code.

5.9.51 Scan Code Enable Register — Index 99h

Bit	Name	R/W	Reset	Default	Description
7	SCAN_EN7	R/W	3VA	1	Set “1” to enable GPIO67 scan code function.
6	SCAN_EN6	R/W	3VA	1	Set “1” to enable GPIO66 scan code function.
5	SCAN_EN5	R/W	3VA	1	Set “1” to enable GPIO65 scan code function.
4	SCAN_EN4	R/W	3VA	1	Set “1” to enable GPIO64 scan code function.
3	SCAN_EN3	R/W	3VA	1	Set “1” to enable GPIO63 scan code function.

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2	SCAN_EN2	R/W	3VA	1	Set “1” to enable GPIO62 scan code function.
1	SCAN_EN1	R/W	3VA	1	Set “1” to enable GPIO61 scan code function.
0	SCAN_EN0	R/W	3VA	1	Set “1” to enable GPIO60 scan code function.

5.9.52 Break Code Enable Register — Index 9Ah

Bit	Name	R/W	Reset	Default	Description
7	BREAK_EN7	R/W	3VA	1	0: No break asserted when GPIO67 is released. (rising edge) 1. Break code is asserted when GPIO67 is released.
6	BREAK_EN6	R/W	3VA	1	0: No break asserted when GPIO66 is released. (rising edge) 1. Break code is asserted when GPIO66 is released.
5	BREAK_EN5	R/W	3VA	1	0: No break asserted when GPIO65 is released. (rising edge) 1. Break code is asserted when GPIO65 is released.
4	BREAK_EN4	R/W	3VA	1	0: No break asserted when GPIO64 is released. (rising edge) 1. Break code is asserted when GPIO64 is released.
3	BREAK_EN3	R/W	3VA	1	0: No break asserted when GPIO63 is released. (rising edge) 1. Break code is asserted when GPIO63 is released.
2	BREAK_EN2	R/W	3VA	1	0: No break asserted when GPIO62 is released. (rising edge) 1. Break code is asserted when GPIO62 is released.
1	BREAK_EN1	R/W	3VA	1	0: No break asserted when GPIO61 is released. (rising edge) 1. Break code is asserted when GPIO61 is released.
0	BREAK_EN0	R/W	3VA	1	0: No break asserted when GPIO60 is released. (rising edge) 1. Break code is asserted when GPIO60 is released.

5.9.53 Prefix Code Enable Register — Index 9Bh

Bit	Name	R/W	Reset	Default	Description
7	PRE_CODE_EN7	R/W	3VA	1	0: No prefix code before make/break code for GPIO67. 1. Prefix code is asserted before make/break code for GPIO67.
6	PRE_CODE_EN6	R/W	3VA	1	0: No prefix code before make/break code for GPIO66. 1. Prefix code is asserted before make/break code for GPIO66.
5	PRE_CODE_EN5	R/W	3VA	1	0: No prefix code before make/break code for GPIO65. 1. Prefix code is asserted before make/break code for GPIO65.
4	PRE_CODE_EN4	R/W	3VA	1	0: No prefix code before make/break code for GPIO64. 1. Prefix code is asserted before make/break code for GPIO64.
3	PRE_CODE_EN3	R/W	3VA	1	0: No prefix code before make/break code for GPIO63. 1. Prefix code is asserted before make/break code for GPIO63.
2	PRE_CODE_EN2	R/W	3VA	1	0: No prefix code before make/break code for GPIO62. 1. Prefix code is asserted before make/break code for GPIO62.
1	PRE_CODE_EN1	R/W	3VA	1	0: No prefix code before make/break code for GPIO61. 1. Prefix code is asserted before make/break code for GPIO61.
0	PRE_CODE_EN0	R/W	3VA	1	0: No prefix code before make/break code for GPIO60. 1. Prefix code is asserted before make/break code for GPIO60.

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5.9.54 Make Code Register 0 — Index 9Ch (SCAN_BANK_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE0	R/W	3VA	0	Make code for GPIO60. When GPIO60 is pressed (falling edge), this code is asserted via KBC. When GPIO60 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.55 Make Code Register 1 — Index 9Ch (SCAN_BANK_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE1	R/W	3VA	0	Make code for GPIO61. When GPIO61 is pressed (falling edge), this code is asserted via KBC. When GPIO61 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.56 Make Code Register 2 — Index 9Ch (SCAN_BANK_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE2	R/W	3VA	0	Make code for GPIO62. When GPIO62 is pressed (falling edge), this code is asserted via KBC. When GPIO62 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.57 Make Code Register 3 — Index 9Ch (SCAN_BANK_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE3	R/W	3VA	0	Make code for GPIO63. When GPIO63 is pressed (falling edge), this code is asserted via KBC. When GPIO63 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.58 Make Code Register 4 — Index 9Ch (SCAN_BANK_SEL = 4)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE4	R/W	3VA	0	Make code for GPIO60. When GPIO64 is pressed (falling edge), this code is asserted via KBC. When GPIO64 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.59 Make Code Register 5 — Index 9Ch (SCAN_BANK_SEL = 5)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE5	R/W	3VA	0	Make code for GPIO65. When GPIO65 is pressed (falling edge), this code is asserted via KBC. When GPIO65 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

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5.9.60 Make Code Register 6 — Index 9Ch (SCAN_BANK_SEL = 6)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE6	R/W	3VA	0	Make code for GPIO66. When GPIO66 is pressed (falling edge), this code is asserted via KBC. When GPIO66 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.61 Make Code Register 7 — Index 9Ch (SCAN_BANK_SEL = 7)

Bit	Name	R/W	Reset	Default	Description
7-0	MAKE_CODE7	R/W	3VA	0	Make code for GPIO67. When GPIO67 is pressed (falling edge), this code is asserted via KBC. When GPIO67 is released (rising edge), this code + 0x80 (i.e. break code) is asserted via KBC.

5.9.62 Prefix Code Register 0 — Index 9Dh (SCAN_BANK_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE0	R/W	3VA	E0h	Prefix code for GPIO60. This code is asserted before make/break code.

5.9.63 PRE Code Register 1 — Index 9Dh (SCAN_BANK_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE1	R/W	3VA	E0h	Prefix code for GPIO61. This code is asserted before make/break code.

5.9.64 PRE Code Register 2 — Index 9Dh (SCAN_BANK_SEL = 2)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE2	R/W	3VA	E0h	Prefix code for GPIO62. This code is asserted before make/break code.

5.9.65 PRE Code Register 3 — Index 9Dh (SCAN_BANK_SEL = 3)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE3	R/W	3VA	E0h	Prefix code for GPIO63. This code is asserted before make/break code.

5.9.66 PRE Code Register 4 — Index 9Dh (SCAN_BANK_SEL = 4)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE4	R/W	3VA	E0h	Prefix code for GPIO64. This code is asserted before make/break code.

5.9.67 PRE Code Register 0 — Index 9Dh (SCAN_BANK_SEL = 5)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE5	R/W	3VA	E0h	Prefix code for GPIO65. This code is asserted before make/break code.

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5.9.68 PRE Code Register 6 — Index 9Dh (SCAN_BANK_SEL = 6)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE6	R/W	3VA	E0h	Prefix code for GPIO66. This code is asserted before make/break code.

5.9.69 PRE Code Register 7 — Index 9Dh (SCAN_BANK_SEL = 7)

Bit	Name	R/W	Reset	Default	Description
7-0	PRE_CODE7	R/W	3VA	E0h	Prefix code for GPIO67. This code is asserted before make/break code.

5.9.70 Make Code Status Register — Index 9Eh

Bit	Name	R/W	Reset	Default	Description
7	SCAN7_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO67. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN7_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
6	SCAN6_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO66. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN6_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
5	SCAN5_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO65. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN5_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
4	SCAN4_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO64. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN4_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
3	SCAN3_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO63. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN3_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
2	SCAN2_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO62. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN2_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.

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1	SCAN1_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO61. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN1_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.
0	SCAN0_MAKE_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of make code by GPIO60. When KeyBoard Key emulation event occurs and the make code of this key is sent, this bit will be set to 1. SCAN0_MAKE_STS will be cleared after host reading IO port 0x0060. The status will continue to occur when the key is pressed. Delay time and repeat time are determined by REP_TIME and REP_DEL_TIME.

5.9.71 Break Code Status Register — Index 9Fh

Bit	Name	R/W	Reset	Default	Description
7	SCAN7_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO67. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN7_BRK_STS will be cleared after host reading IO port 0x0060.
6	SCAN6_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO66. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN6_BRK_STS will be cleared after host reading IO port 0x0060.
5	SCAN5_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO65. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN5_BRK_STS will be cleared after host reading IO port 0x0060.
4	SCAN4_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO64. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN4_BRK_STS will be cleared after host reading IO port 0x0060.
3	SCAN3_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO63. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN3_BRK_STS will be cleared after host reading IO port 0x0060.
2	SCAN2_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO62. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN2_BRK_STS will be cleared after host reading IO port 0x0060.
1	SCAN1_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO61. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN1_BRK_STS will be cleared after host reading IO port 0x0060.
0	SCAN0_BRK_STS	R/W	LRESET#	0	The KeyBoard Key emulation status of break code by GPIO60. When KeyBoard Key emulation event occurs and the break code of this key is sent, this bit will be set to 1. SCAN0_BRK_STS will be cleared after host reading IO port 0x0060.

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5.9.72 GPIO7 Output Enable Register — Index 80h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_OE	R/W	LRESET#	0	0: GPIO77 is in input mode. 1: GPIO76 is in output mode.
6	GPIO76_OE	R/W	LRESET#	0	0: GPIO76 is in input mode. 1: GPIO76 is in output mode.
5	GPIO75_OE	R/W	LRESET#	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	LRESET#	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	LRESET#	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	LRESET#	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	LRESET#	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	LRESET#	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

5.9.73 GPIO7 Output Data Register — Index 81h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_VAL	R/W	LRESET#	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_VAL	R/W	LRESET#	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_VAL	R/W	LRESET#	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_VAL	R/W	LRESET#	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_VAL	R/W	LRESET#	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_VAL	R/W	LRESET#	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.
1	GPIO71_VAL	R/W	LRESET#	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_VAL	R/W	LRESET#	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

5.9.74 GPIO7 Pin Status Register — Index 82h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_IN	R	-	-	The pin status of GPIO77.
6	GPIO76_IN	R	-	-	The pin status of GPIO76.

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5	GPIO75_IN	R	-	-	The pin status of GPIO75.
4	GPIO74_IN	R	-	-	The pin status of GPIO74.
3	GPIO73_IN	R	-	-	The pin status of GPIO73.
2	GPIO72_IN	R	-	-	The pin status of GPIO72.
1	GPIO71_IN	R	-	-	The pin status of GPIO71.
0	GPIO70_IN	R	-	-	The pin status of GPIO70.

5.9.75 GPIO7 Drive Enable Register — Index 83h

Bit	Name	R/W	Reset	Default	Description
7	GPIO77_DRV_EN	R/W	LRESET#	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.
6	GPIO76_DRV_EN	R/W	LRESET#	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.
5	GPIO75_DRV_EN	R/W	LRESET#	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	LRESET#	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.
3	GPIO73_DRV_EN	R/W	LRESET#	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	LRESET#	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	LRESET#	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	LRESET#	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

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5.10 Watch Dog Timer Registers (LDN 0x07)

5.10.1 WDT Device Base Address Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	WDT_EN	R/W	LRESET#	0	0: disable WDT base address. 1: enable WDT base address.

5.10.2 Base Address High Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_HI	R/W	LRESET#	00h	The MSB of WDT base address.

5.10.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7-0	BASE_ADDR_LO	R/W	LRESET#	00h	The LSB of WDT base address.

5.10.4 Watchdog Output Enable Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	WDOUT_EN	R/W	3VA	0	0: disable Watchdog time out output via WDTRST#. 1: enable Watchdog time out output via WDTRST#.
6-1	Reserved	-	-	-	Reserved

5.10.5 Watchdog Control Configuration Register 1 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7	WD_CLK_SEL	R/W	3VA	0	0: Watchdog timer clock is 10Hz clock divided by CLKIN. 1: Watchdog timer clock is internal 10Hz clock.
6	WDTMOUT_STS	R/W	3VA	0	If watchdog timeout event occurred, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	3VA	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	3VA	1	Select output mode (0: level, 1: pulse) of WDTRST# by setting this bit.
3	WD_UNIT	R/W	3VA	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	3VA	0	Select output polarity of WDTRST# (1: high active, 0: low active) by setting this bit.
1-0	WD_PSWIDTH	R/W	3VA	10b	Select output pulse width of WDTRST# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

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5.10.6 Watchdog Timer Configuration Register 2 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME	R/W	3VCC	5h	Time of watchdog timer (0~255)

5.10.7 Watchdog PME Enable Configuration Register 2 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME	R	3VA	-	The PME Status. This bit will set when WDT_PME_EN is set and the watchdog timer is 1 unit before time out (or time out).
6	WDT_PME_EN	R/W	3VA	0	0: Disable Watchdog PME. 1: enable Watchdog PME.
5	WDT_PME_ST	R/WC	3VA	0	When WDT_PME occurs, this bit will be set. Write “1” to clear.
4-1	Reserved	-		-	Reserved.
0	CPU_CHG_STS	R/W	VBAT	0	This bit will be set at rising edge of pin 55. Write “1” to clear.

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5.11 PME, ACPI, and ERP Power Saving Registers (LDN 0x0A)

5.11.1 PME Device Enable Register — Index 30h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	-	-	-	Reserved
0	PME_EN	R/W	3VA	0	PME global enable register. 0: disable PME. 1: enable PME.

5.11.2 ERP Enable Register — Index E0h

Bit	Name	R/W	Reset	Default	Description
7	ERP_EN	R/W	VBAT	0	0: disable ERP function 1: enable ERP function
6	S3_BACK	R/W	VBAT	0	This bit will set “1” when system is back from S3 state.
5-2	Reserved	R/W	VBAT	0	Reserved
1	ERP_PME_EN	R/W	VBAT	0	PME event enable. 0: disable PME event. 1: enable PME event, when wakeup event detected.
0	ERP_PSOUT_EN	R/W	VBAT	0	PSOUT# event enable. This bit has no function if ERP_PME_EN is set. 0: disable RING1 PSOUT# event. 1: enable RING1 PSOUT# event, when wakeup event detected.

5.11.3 ERP Control Register 1 — Index E1h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	R/W	VBAT	11b	Reserved for Fintek test mode.
5	S3_ ERP_CTRL1#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL1# will output Low when S3 state. Else If set to “1” ERP_CTRL1# will output High when S3 state.
4	S3 _ ERP_CTRL0#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL0# will output Low when S3 state. Else If set to “1” ERP_CTRL0# will output High when S3 state.
3	S5 _ ERP_CTRL1#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL1# will output Low when S5 state. Else If set to “1” ERP_CTRL1# will output High when S5 state.
2	S5 _ ERP_CTRL0#_DIS	R/W	VBAT	1	If clear to “0” ERP_CTRL0# will output Low when S5 state. Else If set to “1” ERP_CTRL0# will output High when S5 state.
1	AC_ ERP_CTRL1#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL1# will output Low when after AC lost. Else If set to “1” ERP_CTRL1# will output High when after AC lost.
0	AC_ ERP_CTRL0#_DIS	R/W	VBAT	0	If clear to “0” ERP_CTRL0# will output Low when after AC lost. Else If set to “1” ERP_CTRL0# will output High when after AC lost.

5.11.4 ERP Control Register 2 — Index E2h

Bit	Name	R/W	Reset	Default	Description

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7	AC_LOST	R/WC	3VA	1	This bit is AC lost status and writes 1 to this bit will clear it.
6	Reserved	R/W	VBAT	0	Dummy register
5	CTRL1#_RSMRST_EN	R/W	VBAT	0	0: Disable ERP_CTRL1# assert RSMRST low 1: Enable ERP_CTRL1# assert RSMRST low
4	CTRL0#_RSMRST_EN	R/W	VBAT	0	0: Disable ERP_CTRL0# assert RSMRST low 1: Enable ERP_CTRL0# assert RSMRST low
3-2	Reserved	R/W	VBAT	0	Dummy register.
1	RSMRST_DET_5V_DIS	R/W	VBAT	0	Device detects 5VA power ok (4.4V) and 3VSB become high, and after ~50ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check 5VA power ok.
0	Reserved	R	VBAT	0	Dummy register.

5.11.5 ERP PSIN De-bounce Register — Index E3h

Bit	Name	R/W	Reset	Default	Description
7-0	PSIN_DEB_TIME	R/W	VBAT	13h	PSIN# pin input de-bounce time. The unit is 1ms, default is 20ms.

5.11.6 ERP RSMRST De-bounce Register — Index E4h

Bit	Name	R/W	Reset	Default	Description
7-0	RSMRST_DEB_TIME	R/W	VBAT	9h	RSMRST internal de-bounce time. The unit is 1ms and default is 10ms.

5.11.7 ERP PSOUT Pulse Width Register — Index E5h

Bit	Name	R/W	Reset	Default	Description
7-0	PS_OUT_PW	R/W	VBAT	C7h	PS_OUT output pulse width. The unit is 1ms and default is 200ms.

5.11.8 ERP PSIN De-bounce Register — Index E6h (Powered by VBAT)

Bit	Name	R/W	Reset	Default	Description
7-0	PSON_DEB_TIME	R/W	VBAT	9h	PS_ON# pin input de-bounce time. The unit is 1ms, default is 10ms.

5.11.9 ERP Deep S5 Delay Register — Index E7h

Bit	Name	R/W	Reset	Default	Description
7-0	DS5_DELAY_TIME	R/W	VBAT	63h	The delay time from S5 state to deep S5 state. The unit is 64ms and default is 6.4 sec. Deep S5 state will disable if this byte is “0”. Write “0h” to this byte will disable deep S5.

5.11.10 ERP Wakeup Enable Register — Index E8h

Bit	Name	R/W	Reset	Default	Description
7	RI2_WAKEUP_EN	R/W	VBAT	0	Enable RI2# PME# event to wakeup.
6	Reserved	R/W	VBAT	0	Dummy register.

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5	RI1_WAKEUP_EN	R/W	VBAT	0	Enable RI1# PME# event to wakeup.
4	RING_WAKEUP_EN	R/W	VBAT	1	Set this bit to enable EVENT_IN# event to wakeup system.
3	GP_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable GPIO event to wakeup system.
2	TMOUT_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Timeout event to wakeup system.
1	MO_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Mouse event to wakeup system.
0	KB_WAKEUP_EN	R/W	VBAT	0	Set this bit to enable Keyboard event to wakeup system.

5.11.11 ERP Deep S3 Delay Register — Index E9h

Bit	Name	R/W	Reset	Default	Description
7-0	DS3_DELAY_TIME	R/W	VBAT	Fh	The delay time from S3 state to deep S3 state. The unit is 64ms and default is 1.024 sec. Deep S3 state will disable if this byte is “0”. Write “0h” to this byte will disable deep S3.

5.11.12 ERP Mode Select Register — Index ECh

Bit	Name	R/W	Reset	Default	Description
7-6	ERP_MODE	R/W	VBAT	0	00: Fintek G3’ mode. 01: Intel DSW + Fintek G3` mode. 10: Reserved. 11: Intel DSW mode.
5	DPWROK_EN	R/W	VBAT	0	0: disable ERP_CTRL1# assert DPWROK low 1: enable ERP_CTRL 1# assert DPWROK low
4-0	Revered	-	-	-	Reserved.

5.11.13 ERP WDT Control Register — Index EDh

Bit	Name	R/W	Reset	Default	Description
7-6	WDT_TIME[11:10]	R/W	VBAT	0	Bit 11 and 10 of WDT_TIME
5	Revered	-	-	-	Reserved.
4	WD_TMOUT	R/W	VBAT	-	ERP watchdog timer timeout status. Write 1 to clear.
3-2	WDT_TIME[9:8]	R/W	VBAT	0	Bit 9 and 8 of WDT_TIME
1	WD_UNIT	R/W	VBAT	0	0: unit of WD_TIME is 1 sec. 1: unit of WD_TIME is 1 minute.
0	WD_EN	R/W	VBAT	0	Enable ERP watchdog timer.

5.11.14 ERP WDT Time Register — Index EEh

Bit	Name	R/W	Reset	Default	Description
7-0	WD_TIME[7:0]	R/W	VBAT	0	ERP watchdog timer count time register. Start to count down when WD_EN is set. When reaching 0, WD_EN will auto clear and WD_TMOUT is set. A wakeup event will assert if enabled

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5.11.15 PME Event Enable 1 Register — Index F0h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME_EN	R/W	3VA	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
6	MO_PME_EN	R/W	3VA	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
5	KB_PME_EN	R/W	3VA	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	3VA	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3	PRT_PME_EN	R/W	3VA	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
2	UR2_PME_EN	R/W	3VA	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
1	UR1_PME_EN	R/W	3VA	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.
0	Reserved	-	-	-	Reserved.

5.11.16 PME Event Status 1 Register — Index F1h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PME_ST	R/WC	3VA	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	MO_PME_ST	R/WC	3VA	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/WC	3VA	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/WC	3VA	-	Hardware monitors PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.

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3	PRT_PME_ST	R/WC	3VA	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UR2_PME_ST	R/WC	3VA	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UR1_PME_ST	R/WC	3VA	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	Reserved	-	-	-	Reserved.

5.11.17 PME Event Enable 2 Register — Index F2h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved.
2	RI2_PME_EN	R/W	3VA	0	RI2# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.
1	RI1_PME_EN	R/W	3VA	0	RI1# PME event enable. 0: disable RI1# PME event. 1: enable RI1# PME event.
0	GPIO_PME_EN	R/W	3VA	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.

5.11.18 PME Event Status 2 Register — Index F3h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3	ERP_PME_ST	R/WC	3VA	-	ERP PME event status. 0: ERP has no PME event. 1: ERP has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	RI2_PME_ST	R/WC	3VA	-	RI2# PME event status. 0: RI2# has no PME event. 1: RI2# has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	RI1_PME_ST	R/WC	3VA	-	RI1# PME event status. 0: RI1# has no PME event. 1: RI1# has a PME event to assert. Write 1 to clear to be ready for next PME event.

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0	GP_PME_ST	R/WC	3VA	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.

5.11.19 ACPI Control Register 1 — Index F4h

Bit	Name	R/W	Reset	Default	Description
7	TS3	R/W	VBAT	0	Reserved for Fintek Internal Used only.
6	LAST_ST_MODE	R/W	VBAT	0	0: Last state is sampled by PWROK and RSMRST#. 1: Last state is sampled 1 second before AC lost.
5	EN_GPWAKEUP	R/W	VBAT	0	Set one to enable GPIO wakeup event asserted via PSOUT#.
4	EN_KBWAKEUP	R/W	VBAT	0	Set one to enable keyboard wakeup event asserted via PSOUT#.
3	EN_MOWAKEUP	R/W	VBAT	0	Set one to enable mouse wakeup event asserted via PSOUT#.
2-1	PWRCTRL	R/W	VBAT	11	The ACPI Control the PS_ON# to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/WC	3VA	1	When 3VA power lost, it will set to 1, and write 1 to clear it

5.11.20 ACPI Control Register 2 — Index F5h

Bit	Name	R/W	Reset	Default	Description
7-6	PWROK_DELAY	R/W	VBAT	10b	The additional PWROK delay. 00: no delay 01: 100ms. 10: 200ms (default) 11: 400ms.
5	RSTCON_EN	R/W	VBAT	0	0: RSTCON# asserts via PWROK. 1: RSTCON# asserts via PCI_RST4# and PCI_RST5#.
4-3	VDD_DELAY	R/W	3VA	01b	The PWROK delay timing from 3VCCOK by following setting: 00 : 100ms 01 : 200ms (default) 10 : 300ms 11 : 400ms
2	Reserved	-	-	-	Reserved
1	LRESET_DB_EN	R/W	3VA	0	Enable the LRESET# de-bounce. (200us)
0	WDT_DEF_DIS	R/W	3VA	0	0: WDT enable is determined by power on strap. 1: WDT default is disabled.

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5.11.21 ACPI Control Register 3 — Index F6h

Bit	Name	R/W	Reset	Default	Description
7	S3_SEL	R/W	3VA	0	Select the KBC S3 condition source. 0: Enter S3 state when internal 3VCCOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	PS_ON_DEL_EN	R/W	3VA	0	0: PS_ON# is the inverted of S3# signal. 1: PS_ON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
5	OVP_KBRST_EN	R/W	3VA	0	Set “1” to force KBRST# low when OVP/UVP occurs.
4	PCI_RST5_GATE	R/W	3VA	1	Write “0” to this bit will force PCI_RST5# to sink low.
3	PCI_RST4_GATE	R/W	3VA	1	Write “0” to this bit will force PCI_RST4# to sink low.
2	PCI_RST3_GATE	R/W	3VA	1	Write “0” to this bit will force PCI_RST3# to sink low.
1	PCI_RST2_GATE	R/W	3VA	1	Write “0” to this bit will force PCI_RST2# to sink low.
0	PCI_RST1_GATE	R/W	3VA	1	Write “0” to this bit will force PCI_RST1# to sink low.

5.11.22 ACPI Control Register 4 — Index F7h

Bit	Name	R/W	Reset	Default	Description
7	VDIMM_S3_ON	R/W	VBAT	1	0: VDIMM_EN is low in S3 state. 1: VDIMM_EN is high is S3 state.
6	VDDA_S3_ON	R/W	VBAT	0	0: VDDA_EN is low in S3 state. 1: VDDA_EN is high is S3 state.
5	VCORE_S3_ON	R/W	VBAT	0	0: VCORE_EN is low in S3 state. 1: VCORE_EN is high is S3 state.
4	VLDT_S3_ON	R/W	VBAT	0	0: VLDT_EN is low in S3 state. 1: VLDT_EN is high is S3 state.
3	WDT_PWROK_EN	R/W	VBAT	0	Set “1” to enable WDTRST# & assert via PWROK.
2	S0P5_GATE_S5_ST	R/W	VBAT	1	0: S0P5_GATE# is low in S5 state. 1: S0P5_GATE# is high in S5 state.
1	S3P5_GATE_S5_ST	R/W	VBAT	1	0: S3P5_GATE# is low in S5 state. 1: S3P5_GATE# is high in S5 state.
0	RSTCON_MODE	R/W	VBAT	0	0: Level mode. 1: Pulse mode, falling edge will assert a 250ms low pulse.

5.11.23 LED_VCC Control Register — Index F8h

Bit	Name	R/W	Reset	Default	Description
7	LED_VCC_INV_DIS	R/W	VBAT	0	Invert LED_VCC clock output.
6	LED_VCC_DS3	R/W	VBAT	0	Enable LED_VCC deep S3 mode. LED_VCC will output 0.25Hz clock with 75% duty when enter deep S3 state.

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5-4	LED_VCC_S5_MODE	R/W	VBAT	0	Select LED_VCC mode in S5 state. The mode is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VCC_S3_MODE	R/W	VBAT	0	Select LED_VCC mode in S3 state. The mode is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VCC_S0_MODE	R/W	VBAT	0	Select LED_VCC mode in S0 state. The mode is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

5.11.24 LED_VSB Control Register — Index F9h

Bit	Name	R/W	Reset	Default	Description
7	WDT_PCI_RST4_EN	R/W	VBAT	0	Set “1” to enable WDTRST# assert via PCI_RST4#.
6	LED_VSB_DS3	R/W	VBAT	0	Enable LED_VSB deep S3 mode. LED_VSB will output 0.25Hz clock with 75% duty when enter deep S3 state.

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5-4	LED_VSB_S5_MODE	R/W	VBAT	0	Select LED_VSB mode in S5 state. The mode is controlled by {LED_VSB_S5_ADD, LED_VSB_S5_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
3-2	LED_VSB_S3_MODE	R/W	VBAT	0	Select LED_VSB mode in S3 state. The mode is controlled by {LED_VSB_S3_ADD, LED_VSB_S3_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.
1-0	LED_VSB_S0_MODE	R/W	VBAT	0	Select LED_VSB mode in S0 state. The mode is controlled by {LED_VSB_S0_ADD, LED_VSB_S0_MODE} 000: Sink low. 001: Tri-state. 010: 0.5Hz clock. 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 75% duty. 111: 0.25Hz clock with 75% duty.

5.11.25 LED Additional Control Register — Index FAh

Bit	Name	R/W	Reset	Default	Description
7	LED_VSB_DRV_EN	R/W	VBAT	0	0: LED_VSB is open drain. 1: LEC_VSB is push-pull.
6	LED_VSB_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S5_MODE.
5	LED_VSB_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S3_MODE.
4	LED_VSB_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VSB_S0_MODE.
3	LED_VCC_DRV_EN	R/W	VBAT	0	0: LED_VCC is open drain. 1: LEC_VCC is push-pull.
2	LED_VCC_S5_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S5_MODE.
1	LED_VCC_S3_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S3_MODE.

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0	LED_VCC_S0_MODE_ADD	R/W	VBAT	0	Refer to LED_VCC_S0_MODE.

5.11.26 ACPI Control Register 5 — Index FBh

Bit	Name	R/W	Reset	Default	Description
7	PSIN_FLAG	R/W	3VA	0	This bit will set “1” when PSIN# is pressed over the time set by PSIN_DET_SEL. Write “1” to clear this bit.
6	Reserved	R/W	3VA	0	Dummy register.
5	PWROK_VDD_DIS	R/W	3VA	0	PWROK will not refer to 3VCC power good signal when this bit is set.
4	ABNORMAL_PSOUT_EN	R/W	3VA	0	When this bit is set, PWROK drop in S0 state will assert a 250ms low pulse via PSOUT# to shut down system.
3	Reserved	R/W	VBAT	0	Dummy register.
2-1	PSIN_DET_SEL	R/W	VBAT	00b	Time for PSIN_FLAG. 00: 1 sec. 01: 2 sec. 10: 3 sec. 11: 4 sec.
0	PSNI_DET_EN	R/W	VBAT	0	Set “1” to enable detecting PSIN# during power on.

5.11.27 ACPI Control Register 6 — Index FCh

Bit	Name	R/W	Reset	Default	Description
7	WDT_MODE	R/W	3VA	0	0: WDT assert once, WDT will disable after asserting WDTRST#. 1: Auto reload mode, WDT is disabled by software, timer will be reload after timeout occurs.
6	OVP_DLY_MODE	R/W	3VA	0	0: Force mode has no delay. 1: Force mode has delay as alarm mode.
5	S3P5_GATE_S3_ST	R/W	3VA	0	0: S3P5_GATE# is low in S3 state. 1: S3P5_GATE# is high in S3 state.
4	S0P5_GATE_S3_ST	R/W	3VA	1	0: S0P5_GATE# is low in S3 state. 1: S0P5_GATE# is high in S3 state.
3-0	DSW_DELAY	R/W	3VA	0111b	This is the delay time between SUS_WARN# and SUS_ACK#. The unit is 0.5 sec. Default time is 3.5s ~ 4s. The default could be trimmed to 0s ~ 0.5s.

5.11.28 RI# De-bounce Select Register — Index FEh

Bit	Name	R/W	Reset	Default	Description
7-5	Reserved	-	-	-	Reserved for Fintek test mode. Don’t write “1” to this register.
4-2	Reserved	-	-	-	Reserved.
1-0	RI_DB_SEL	R/W	3VA	0	Select RI de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

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6 Hardware Monitor Registers

6.1 Overviews

Below registers could be accessed by I²C & LPC. Please refer to the register for more detail information:

Register CR01 ~ CR03 → Configuration Registers
Register CR04 → Debug Port Temperature Select Register
Register CR06 → I2C Slave Address Register
Register CR07 → MXM Address Register
Register CR08 → TSI Address Register
Register CR09 → SMBus Master Address Register
Register CR0A ~ CR0F → PECI/MXM/TSI Control Register 1~6
Register CR10 ~ CR37 → Voltage Setting Register
Register CR40 ~ CR4F → PECI 3.0 Command and Register
Register CR50 ~ CR5F → TSI/MXM Setting Register
Register CR60 ~ CR8E → Temperature Setting Register
Register CR90 ~ CRDF → Fan Control Setting Register
→Fan1 Detail Setting CRA0 ~ CRAF
→Fan2 Detail Setting CRB0 ~ CRBF
→Fan3 Detail Setting CRC0 ~ CRCF

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6.2 Configuration Registers

6.2.1 Configuration Register 1— Index 01h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	0h	-	0	Reserved
2	POWER_DOWN	R/W	3VA	0	Hardware monitor function power down function.
1	FAN_START	R/W	3VA	1	1: enable startup of fan monitoring operations. 0: Put the part in the standby mode.
0	V_T_START	R/W	3VA	1	1: enable startup of temperature and voltage monitoring operations 0: Put the part in the standby mode.

6.2.2 Configuration Register 2 — Index 02h

Bit	Name	R/W	Reset	Default	Description
7	TSI_RST_SEL	R/W	3VA	1	0: MXM/TSI/PECI enable registers reset by LRESET#. 1: MXM/TSI/PECI enable registers reset by VDD3VOK. Affected registers are MXM_EN, TSI_EN and PECI_EN.
6	CASE_BEEP_EN	R/W	3VA	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	3VA	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	HM_S3_MON_EN	R/W	3VA	0	0: Monitor voltage/temperature in S0 state only. 1: Monitor voltage/temperature in S0/S3/S5 state.
2	CASE_SMI_EN	R/W	3VA	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	3VA	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

6.2.3 Configuration Register 3 — Index 03h

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	R/W	-	0	Reserved
0	CASE_STS	R/W	VBAT	0	Case open event status write 1 to clear if case open event cleared. (This bit is powered by VBAT.)

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6.3 Debug Port Temperature Select Register

6.3.1 Debug Port Temperature Select Register— Index 04h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	R/W	3VA	0	Reserved registers.
3	Reserved	-	-	-	Reserved
2-0	DPORT_TEMP_SEL	R/W	3VA	1	0h: Reserved. 1h: Diode 1 reading. 2h: Diode 2 reading. 3h: Diode 3 reading. 4h: TSI reading. 5h: MXM reading. 6h: Reserved. 7h: PECI reading.

6.3.2 DTS I/F S3 Control Register — Index 05h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	-	-	-	Reserved
2-0	Reserved	R/W	3VA	0	Reserved registers.

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6.4 I²C Address Register

6.4.1 I2C Slave Address Register — Index 06h

Bit	Name	R/W	Reset	Default	Description
7-1	I2C_ADDR	R/W	3VA	2Eh	Address sent for I2C Slave. I2C master could use this address to access Hardware monitor and configuration registers.
0	Reserved	-	-	-	Reserved

6.4.2 MXM Address Register — Index 07h

Bit	Name	R/W	Reset	Default	Description
7-1	MXM_ADDR	R/W	3VA	25h	Address sent for MXM protocol.
0	Reserved	-	-	-	Reserved

6.4.3 TSI Address Register — Index 08h

Bit	Name	R/W	Reset	Default	Description
7-1	TSI_ADDR	R/W	3VA	26h	Address sent for AMD TSI protocol.
0	Reserved	-	-	-	Reserved

6.4.4 SMBus Master Address Register — Index 09h

Bit	Name	R/W	Reset	Default	Description
7-1	SMBUS_ADDR	R/W	3VA	0	Address sent by embedded SMBus master.
0	Reserved	R/W	-	0	Reserved

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6.5 Digital Temperature Control Register

6.5.1 PECI/MXM/TSI Control Register 1 — Index 0Ah

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	MXM_BYTE_MODE	R/W	3VA	0	0: MXM is accessed by block read protocol. 1: MXM is accessed by send byte / receive byte protocol.
5	Reserved	-	-	-	Reserved
4	MXM_EN	R/W	VDD3VOK/ LRESET#	0	0: Disable MXM access. 1: Enable MXM access.
3-2	VTT_SEL	R/W	3VA	0	PECI (VTT) voltage selection. 00: VTT is 1.23V 01: VTT is 1.13V 10: VTT is 1.00V 11: VTT is 1.00V
1	TSI_EN	R/W	VDD3VOK/ LRESET#	0	0: Disable AMD TSI access. 1: Enable AMD TSI access.
0	PECI_EN	R/W	VDD3VOK/ LRESET#	0	0: Disable PECI access. 1: Enable PECI access.

6.5.2 PECI/MXM/TSI Control Register 2 — Index 0Bh

Bit	Name	R/W	Reset	Default	Description
7-4	CPU_SEL	R/W	3VA	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping () command to find the CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 0, i.e. PECI address is 0x31. 0100: CPU is in socket 0, i.e. PECI address is 0x32. 1000: CPU is in socket 0, i.e. PECI address is 0x33. Others are reserved.
3-1	Reserved	-	-	0	Reserved.
0	DOMAIN1_EN	R/W	3VA	0	If the CPU is selected as dual core. Set this register 1 to read the temperature of domain1.

6.5.3 PECI/MXM/TSI Control Register 3— Index 0Ch

Bit	Name	R/W	Reset	Default	Description
7-0	TCC_TEMP	R/W	3VA	8'h55	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127°C.

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6.5.4 PECI/MXM/TSI Control Register 4— Index 0Dh

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_OFFSET	R/W	3VA	0	This byte is used as the offset to be added to the CPU temperature reading of AMD_TSI. The range of this register is -128 ~ 127°C.

6.5.5 PECI/MXM/TSI Control Register 5 — Index 0Eh

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_OFFSET	R/W	3VA	0	This byte is used as the offset to be added to the temperature reading of MXM. The range of this register is -128 ~ 127°C.

6.5.6 PECI/MXM/TSI Control Register 6— Index 0Fh

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1-0	DIG_RATE_SEL	R/W	3VA	0	Reserved for Fintek use only

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6.6 Voltage Setting

6.6.1 Voltage-Protect Shut Down Enable Register — Index 10h

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	0	Reserved.
6	V6_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for VIN6
5	V5_VP_EN	R/W	VBAT*	0	Voltage-Protect enable for VIN5
4-2	Reserved	-	-	0	Reserved
1	V1_PME_EN	R/W	3VA	0	VIN1 (Vcore) PME# event enable.
0	VCC_VP_EN	R/W	VBAT*	0	Voltage-Protect shut down enable for 3VCC

*OVP Enable bit is auto clear when OVP event occurs if OVP_MODE is “1” and ALARM_RESET_DIS is “0”

6.6.2 Voltage-Protect Status Register — Index 11h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1	V1_EXC_STS	R/WC	VBAT/ 3VA*	0	This bit is set when V1_EXC is changed. Write “1” to clear this bit.
0	V_EXC_VP	R/WC	VBAT/ 3VA*	0	This bit is voltage-protect status. Once one of the monitored voltages (3VCC, VIN5, VIN6) over its related over-voltage limits or under its related under-voltage limits and if the related voltage-protect shut down enable bit is set, this bit will be set to 1. Write a 1 to this bit will clear it to 0. (This bit is powered by VBAT)

*Reset by VBAT when OVP_MODE is “0”, Reset by 3VA when OVP_MODE is “1”

6.6.3 VIN1 Over Limit Register (Powered by VBAT) — Index 12h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1	V1_EXC	R/WC	3VCC*	0	VIN1 over limit real time status. It is set when VIN1 is over V1_HIGH_LIMIT and clear when VIN1 is under V1_HIGH_LIMIT. This bit is also used to assert BEEP is V1_BEEP_EN is set.
0	Reserved	-	-	0	Reserved.

6.6.4 VIN1 Beep Enable Register — Index 13h

Bit	Name	R/W	Reset	Default	Description
7-2	Reserved	-	-	0	Reserved.
1	V1_BEEP_EN	R/W	3VA	0	VIN1 (Vcore) Beep event enable.
0	Reserved	-	-	0	Reserved.

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6.6.5 Voltage-Protect Configuration Register — Index 16h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	-	Reserved.
3-2	PU_TIME	R/W	VBAT	2'h1	PS_ON# de-active time select in alarm mode of voltage protection. 00: PS_ON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurred. 01: PS_ON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurred. 10: PS_ON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurred. 11: PS_ON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurred.
1-0	VP_EN_DELAY	R/W	VBAT	2'h2	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. 00: bypass 01: 50ms 10: 100ms 11: 200ms

6.6.6 VIN1 Offset Register — Index 3Eh

Bit	Name	R/W	Reset	Default	Description
7-0	V1_OFFSET	R/W	3VA	0	This byte is added to VIN1 reading to present the value in index 0x21. The notation is 2's complement.

6.6.7 Voltage Protection Power Good Select Register — Index 3Fh

Bit	Name	R/W	Reset	Default	Description
7-1	Reserved	--	-	0	Reserved
0	OVP_RST_SEL	R/W	VBAT	0	0: OVP/UVP power good signal is 3VCCOK (3VCC > 2.8V) 1: OVP/UVP power good signal is PWROK. OVP/UVP function wont' start detecting until power good.

6.6.8 Voltage reading and limit— Index 20h- 3Ah

Address	Attribute	Reset	Default Value	Description
20h	R	3VCC	--	3VCC reading. The unit of reading is 8mV.
21h	R	3VCC	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	R	3VCC	--	VIN2 reading. The unit of reading is 8mV.
23h	R	3VCC	--	VIN3 reading. The unit of reading is 8mV.
24h	R	3VCC	--	VIN4 reading. The unit of reading is 8mV.
25h	R	3VCC	--	VIN5 reading. The unit of reading is 8mV.
26h	R	3VCC	--	VIN6 reading. The unit of reading is 8mV.
27h	R	3VCC	--	3VSB reading. The unit of reading is 8mV.
28h	R	3VCC	--	VBAT reading. The unit of reading is 8mV.

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29h	R	3VCC	--	5VA reading. The unit of reading is 8 mV. The 5VA voltage to be monitored is internally divided by 3.
2Ah	R	3VCC	--	3VA reading. The unit of reading is 8mV.
2Bh	R	--	--	Reserved
2Ch	R	3VCC	--	Reserved
2Dh	R	3VCC	--	FAN3 present fan duty reading
2Eh	R	3VCC	--	FAN2 present fan duty reading
2Fh	R	3VCC	--	FAN1 present fan duty reading
30h	R/W	VBAT	89	3VCC under-voltage protection limit. The unit is 8mV
31h	R/W	VBAT	F2	3VCC over-voltage protection limit. The unit is 8mV
32h	R/W	3VA	FF	VIN1 high limit. The unit is 8mv.
32~35h	R		FF	Reserved
36h	R/W	VBAT	E2	VIN5 over-voltage limit (V5_OVV_LIMIT). The unit is 8mv.
37h	R/W	VBAT	E1	VIN6 over-voltage limit (V6_OVV_LIMIT). The unit is 8mv.
38h	R/W	VBAT	83	VIN5 under-voltage limit (V5_UVV_LIMIT). The unit is 8mv.
39h	R/W	VBAT	96	VIN6 under-voltage limit (V6_UVV_LIMIT). The unit is 8mv.

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6.7 PECI 3.0 Command and Register

6.7.1 PECI Configuration Register — Index 40h

Bit	Name	R/W	Reset	Default	Description
7	RDIAMSR_CMD_EN	R/W	3VA	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR() command before a GetTemp() command.
6	C3_UPDATE_EN	R/W	3VA	1	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR() is 0x82.
5-4	Reserved	R	-	-	Reserved
3	C3_PTEMP_EN	R/W	3VA	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is 0x82.
2	C0_PTEMP_EN	R/W	3VA	1	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	3VA	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is 0x82.
0	C0_ALL0_EN	R/W	3VA	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR() is not 0x82 and the bit 8 of completion code is not 1 either.

6.7.2 PECI Master Control Register — Index 41h

Bit	Name	R/W	Reset	Default	Description
7	PECI_CMD_START	W	3VA	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)
6-5	Reserved	R	-	-	Reserved
4	PECI_PENDING	R/W	3VA	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	-	Reserved
2-0	PECI_CMD	R/W	3VA	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

6.7.3 PECI Master Status Register — Index 42h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	-	Reserved
2	ABORT_FCS	R/WC	3VA	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	3VA	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

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0	PECI_FINISH	R/WC	3VA	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

6.7.4 PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA0	R/W	3VA	0	For RdIAMSR(), RdPkgConfig() and WrPkgConfig() command, this byte represents “Host ID[7:1] & Retry[0]”. Please refer to PECI interface specification for more detail.

6.7.5 PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA1	R/W	3VA	0	For RdIAMSR() , this byte represents “Processor ID”. For RdPkgConfig() and WrPkgConfig() , this byte represents “Index”. Please refer to PECI interface specification for more detail.

6.7.6 PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA2	R/W	3VA	0	For RdIAMSR(), this byte is the least significant byte of “MSR Address”. For RdPkgConfig() and WrPkgConfig(), this byte is the least significant byte of “Parameter”. Please refer to PECI interface specification for more detail.

6.7.7 PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA3	R/W	3VA	0	For RdIAMSR(), this byte is the most significant byte of “MSR Address”. For RdPkgConfig() and WrPkgConfig(), this byte is the most significant byte of “Parameter”. Please refer to PECI interface specification for more detail.

6.7.8 PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA4	R/W	3VA	0	For GetDIB() , this byte represents “Device Info” For GetTemp(), this byte represents the least significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte is “Completion Code”. For WrPkgConfig(), this byte represents “DATA[7:0]”

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6.7.9 PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA5	R/W	3VA	0	For GetDIB() , this byte represents “Revision Number” For GetTemp(), this byte represents the most significant byte of temperature. For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[7:0]” For WrPkgConfig(), this byte represents “DATA[15:8]”

6.7.10 PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA6	R/W	3VA	0	For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[15:8]”. For WrPkgConfig(), this byte represents “DATA[23:16]”

6.7.11 PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA7	R/W	3VA	0	For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[23:16]”. For WrPkgConfig(), this byte represents “DATA[31:24]”

6.7.12 PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA8	R/W	3VA	0	For RdIAMSR() and RdPkgConfig() , this byte represents “DATA[31:24]”. For WrPkgConfig(), this byte represents “AW FCS”

6.7.13 PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA9	R/W	3VA	0	For RdIAMSR(), this byte represents “DATA[39:32]”. For WrPkgConfig(), this byte represents “Completion Code”

6.7.14 PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA10	R/W	3VA	0	For RdIAMSR(), this byte represents “DATA[47:40]”.

6.7.15 PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA11	R/W	3VA	0	For RdIAMSR(), this byte represents “DATA[55:48]”.

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6.7.16 PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Reset	Default	Description
7-0	PECI_DATA12	R/W	3VA	0	For RdIAMSR(), this byte represents “DATA[63:56]”.

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6.8 TSI/MXM Temperature Setting

6.8.1 TSI Temperature – Index 50h

Bit	Name	R/W	Reset	Default	Description
7-0	TSI_TEMP	R/W	3VA	-	This is the AMD TSI temperature reading.

6.8.2 MXM Temperature 0 – Index 51h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP0	R/W	3VA	-	This is the high byte of MXM temperature reading. The raw MXM temperature is determined by: MXM_BYTE_MODE is “0”, it is {MXM_TEMP0[0],MXM_TEMP1[7:1]}. MXM_BYTE_MODE is “1”, it is MXM_TEMP0[7:0].

6.8.3 MXM Temperature 1 – Index 52h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP1	R/W	3VA	-	This is the low byte of MXM temperature reading. This byte is not used if MXM_BYTE_MODE is “1”.

6.8.4 MXM Index – Index 53h

Bit	Name	R/W	Reset	Default	Description
7-0	MXM_TEMP_IDX	R/W	3VA	3h	This byte is used for 1. Command sent for MXM protocol if MXM_BYTE_MODE is “0”. 2. Index sent for MXM protocol if MXM_BYTE_MODE is “1”.

6.8.5 SMBus Data 0 – Index 54h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA0	R/W	3VA	8’h00	This is the first byte of the block read/write protocol.

6.8.6 SMBus Data 1 – Index 55h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA1	R/W	3VA	8’h00	This is the second byte of the block read/write protocol.

6.8.7 SMBus Data 2 – Index 56h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA2	R/W	3VA	8’h00	This is the third byte of the block read/write protocol.

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6.8.8 SMBus Data 3 – Index 57h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA3	R/W	3VA	8'h00	This is the 4th byte of the block read/write protocol.

6.8.9 SMBus Data 4 – Index 58h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA4	R/W	3VA	8'h00	This is the 5th byte of the block read/write protocol.

6.8.10 SMBus Data 5 – Index 59h

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA5	R/W	3VA	8'h00	This is the 6th byte of the block read/write protocol.

6.8.11 SMBus Data 6 – Index 5Ah

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA6	R/W	3VA	8'h00	This is the 7th byte of the block read/write protocol.

6.8.12 SMBus Data 7 – Index 5Bh

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_DATA7	R/W	3VA	8'h00	This is the 8th byte of the block read/write protocol.

6.8.13 Block Write Count Register – Index 5Ch

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	-	-	0	Reserved
3-0	BLOCK_WR_CNT	R/W	3VA	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

6.8.14 SMBUS Command Byte/TSI Command Byte – Index 5Dh

Bit	Name	R/W	Reset	Default	Description
7-0	SMBUS_CMD/TSI_CMD	R/W	3VA	0/1	There are actual two bytes for this index. TSI_CMD_PROG select which byte to be programmed: 0: SMBUS_CMD, which is the command code for write byte/word, read byte/word, block write/read and process call protocol. 1: TSI_CMD, which is the command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

6.8.15 SMBUS Status – Index 5Eh

Bit	Name	R/W	Reset	Default	Description

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7	ADC_PENDING	R/W	3VA	0	Set 1 to pending auto TSI/MXM accessing. To use the SCL/ SDA as SMBUS master, set this bit to “1” first.
6	TSI_CMD_PROG	R/W	3VA	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	3VA	0	Kill the current SMBUS transfer and return the state machine to idle. It will set a fail status if the current transfer is not completed.
4	FAIL_STS	R	3VA	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBUS transfer.
3	SMBUS_ABT_ERR	R	3VA	0	This is the arbitration lost status if SMBUS command is issued. Auto cleared by next SMBUS command.
2	SMBUS_TO_ERR	R	3VA	0	This is the timeout status if SMBUS command is issued. Auto cleared by next SMBUS command.
1	SMBUS_NAC_ERR	R	3VA	0	This is the NACK error status if SMBUS command is issued. Auto cleared by next SMBUS command.
0	SMBUS_ READY	R	3VA	1	0: SMBUS transfer is in process. 1: Ready for next SMBUS command.

6.8.16 SMBUS Protocol Select – Index 5Fh

Bit	Name	R/W	Reset	Default	Description
7	SMBUS_START	W	-	0	Write “1” to trigger SMBUS transfer with the protocol specified by SMBUS_PROTOCOL.
6-4	Reserved	-	-	-	Reserved.
3-0	SMBUS_PROTOCOL	R/W	3VA	0	Select what protocol if SMBUS transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: Reserved. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: Reserved Otherwise: reserved.

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6.9 Temperature Register

6.9.1 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Reset	Default	Description
7	EN_ T3_OVT_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_OVT_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_OVT_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	-	-	-	Reserved
3	EN_ T3_EXC_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	3VA	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	-	-	-	Reserved

6.9.2 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Reset	Default	Description
7	T3_OVT_STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP3 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, and write 0 to ignore.
6	T2_OVT _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
5	T1_OVT _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
4	Reserved	-	-	-	Reserved
3	T3_EXC _STS	R/W	3VCC	0	This bit gets 1 to indicate TEMP3 temperature sensor has exceeded high limit or below the “high limit –hysteresis”. Write 1 to clear this bit, write 0 to ignore.
2	T2_EXC _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
1	T1_EXC _STS	R/WC	3VCC	0	This bit gets 1 to indicate TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 to ignore.
0	Reserved	-	-	-	Reserved

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6.9.3 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Reset	Default	Description
7	T3_OVT	R	3VCC	0	Set when the TEMP3 exceeds the OVT limit. Clear when the TEMP3 is below the “OVT limit –hysteresis” temperature.
6	T2_OVT	R	3VCC	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R	3VCC	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	Reserved	-	-	-	Reserved
3	T3_EXC	R	3VCC	0	Set when the TEMP3 exceeds the high limit. Clear when the TEMP3 is below the “high limit –hysteresis” temperature.
2	T2_EXC	R	3VCC	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R	3VCC	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	-	-	-	Reserved

6.9.4 Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Reset	Default	Description
7	EN_T3_OVT_BEEP	R/W	3VA	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_ OVT_BEEP	R/W	3VA	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	3VA	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	Reserved	-	-	-	Reserved
3	EN_ T3_EXC_BEEP	R/W	3VA	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_BEEP	R/W	3VA	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	3VA	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	-	-	-	Reserved

6.9.5 T1 OVT and High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-	-	0	Reserved

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5-4	OVT_TEMP_SEL	R/W	3VA	0	Select the source temperature for T1 OVT Limit. 0: Select T1 to be compared to Temperature 1 OVT Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 OVT Limit. 2: Select CPU temperature from AMD TSI or Intel PCH SMBUS to be compared to Temperature 1 OVT Limit. 3: Select the MAX temperature from Intel PCH SMBUS to be compared to Temperature 1 OVT Limit.
3-2	Reserved	-	-	0	Reserved
1-0	HIGH_ TEMP_SEL	R/W	3VA	0	Select the source temperature for T1 High Limit. 0: Select T1 to be compared to Temperature 1 High Limit. 1: Select CPU temperature from PECI to be compared to Temperature 1 High Limit. 2: Select CPU temperature from AMD TSI or Intel PCH SMBUS to be compared to Temperature 1 High Limit. 3: Select the MAX temperature from Intel PCH SMBUS to be compared to Temperature 1 High Limit.

6.9.6 OVT and Alert Output Enable Register 1 — Index 66h

Bit	Name	R/W	Reset	Default	Description
7	EN_T3_ALERT	R/W	3VA	0	Enable temperature 3 alert event (asserted when temperature over high limit)
6	EN_T2_ALERT	R/W	3VA	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R/W	3VA	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4	Reserved	-	-	-	Reserved.
3	EN_T3_OVT	R/W	3VA	0	Enable over temperature (OVT) mechanism of temperature3.
2	EN_T2_OVT	R/W	3VA	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	3VA	0	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	-	-	-	Reserved.

6.9.7 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	RO	-	0	Reserved
3	T3_MODE	R/W	3VA	1	0: TEMP3 is connected to a thermistor. 1: TEMP3 is connected to a BJT. (default)
2	T2_MODE	R/W	3VA	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	3VA	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	-	-	-	Reserved

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6.9.8 TEMP1 Limit Hystersis Select Register — Index 6Ch

Bit	Name	R/W	Reset	Default	Description
7-4	TEMP1_HYS	R/W	3VA	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	-	-	-	Reserved

6.9.9 TEMP2 and TEMP3 Limit Hystersis Select Register — Index 6Dh

Bit	Name	R/W	Reset	Default	Description
7-4	TEMP3_HYS	R/W	3VA	2h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	TEMP2_HYS	R/W	3VA	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

6.9.10 DIODE OPEN Status Register — Index 6Fh

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6	MXM_OPEN	R	3VCC	-	When MXM interface is enabled, “1” indicates the error of receiving NACK bit or a timeout occurred.
5	PECI_OPEN	R	3VCC	-	When PECI interface is enabled, “1” indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4	TSI_OPEN	R	3VCC	-	When TSI interface is enabled, “1” indicates the error of receiving NACK bit or a timeout occurred.
3	T3_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 3 is open or short
2	T2_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 2 is open or short
1	T1_DIODE_OPEN	R	3VCC	-	“1” indicates external diode 1 is open or short
0	Reserved	-	-	-	Reserved

6.9.11 Temperature — Index 70h- 8Dh

Address	Attribute	Reset	Default Value	Description
70h	Reserved	--	--	Reserved
71h	Reserved	--	--	Reserved
72h	R	3VCC/ 3VA	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	Reserved	--	--	Reserved
74h	R	3VCC/ 3VA	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h	Reserved	--	--	Reserved
76h	R	3VCC/ 3VA	--	Temperature 3 reading. The unit of reading is 1°C.At the moment of reading this register.
77-79h	Reserved	--	--	Reserved

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7Ah	R	3VCC/ 3VA	--	The data of CPU temperature from digital interface after IIR filter. (Available if AMD TSI interface is enabled)
7Bh	R	3VCC/ 3VA	--	The data of MXM temperature from digital interface after IIR filter. (Available if Intel MXM interface is enabled)
7Ch	R	3VCC	--	Reserved
7Dh	R	3VCC	--	Reserved
7Eh	R	3VCC/ 3VA	--	The data of CPU temperature from digital interface after IIR filter. (Available if PECI interface is enabled)
80h	R	3VCC	--	Reserved
81h	R	3VCC	--	Reserved
82h	R/W	3VA	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	3VA	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	3VA	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	3VA	55h	Temperature sensor 2 high limit. The unit is 1°C.
86h	R/W	3VA	64h	Temperature sensor 3 OVT limit. The unit is 1°C.
87h	R/W	3VA	55h	Temperature sensor 3 high limit. The unit is 1°C.
88-8Bh	--	--	--	Reserved
8C~8Dh	--	--	--	Reserved

6.9.12 T1 Slope Adjust Register — Index 7Fh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Reset</th><th>Default</th><th colspan="3">Description</th></tr>
<tr><td>7-4</td><td>Reserved</td><td>-</td><td>-</td><td>-</td><td colspan="3">Reserved</td></tr>
<tr><td>3</td><td>T1_ADD</td><td>R/W</td><td>3VA</td><td>0h</td><td colspan="3">This bit is the sign bit for T1 reading slope adjustment. See T1_SCALE below for detail.</td></tr>
<tr><td>2</td><td>Reserved</td><td>-</td><td>-</td><td>-</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="9">1-0</td><td rowspan="9">T1_SCALE</td><td rowspan="9">R/W</td><td rowspan="9">3VA</td><td rowspan="9">0h</td><td colspan="3"></td></tr>
<tr><td>T1_ADD</td><td>T1_SCALE</td><td>Slope</td></tr>
<tr><td>X</td><td>00</td><td>No adjustment</td></tr>
<tr><td>0</td><td>01</td><td>15/16</td></tr>
<tr><td>0</td><td>10</td><td>31/32</td></tr>
<tr><td>0</td><td>11</td><td>63/64</td></tr>
<tr><td>1</td><td>01</td><td>17/16</td></tr>
<tr><td>1</td><td>10</td><td>33/32</td></tr>
<tr><td>1</td><td>11</td><td>65/64</td></tr>
</table>

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6.10 Fan Control Setting

6.10.1 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	0	Reserved
2	EN_FAN3_PME	R/W	3VA	0	A one enables the corresponding interrupt status bit for PME# interrupt Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	3VA	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	3VA	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

6.10.2 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	R	-	0	Reserved
2	FAN3_STS	R/W	3VCC	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	3VCC	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	3VCC	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

6.10.3 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Reset	Default	Description
7-3	Reserved	--	-	0	Reserved
2	FAN3_EXC	R	3VCC	--	This bit set to high mean that fan3 count can't meet the expected count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	R	3VCC	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	R	3VCC	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.

6.10.4 FAN BEEP Enable Register — Index 93h

Bit	Name	R/W	Reset	Default	Description
7	FULL_WITH_ T3_EN	R/W	3VA	0	Set one will enable FAN to force full speed when T3 over high limit.
6	FULL_WITH_ T2_EN	R/W	3VA	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_ T1_EN	R/W	3VA	0	Set one will enable FAN to force full speed when T1 over high limit.

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4	Reserved	--	-	0	Reserved
3	Reserved	--	-	0	Reserved
2	EN_FAN3_ BEEP	R/W	3VA	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	3VA	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	3VA	0	A one enables the corresponding interrupt status bit for BEEP.

6.10.5 FAN Type Select Register — Index 94h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	--	-	0	Reserved
5-4	FAN3_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL3 0: FANCTRL3 is pull up by external resistor. 1: FANCTRL3 is pull down by internal 100KΩ resistor.
3-2	FAN2_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL2 0: FANCTRL2 is pull up by external resistor. 1: FANCTRL2 is pull down by internal 100KΩ resistor.
1-0	FAN1_TYPE	R/W	3VCC	00	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by FANCTRL1 0: FANCTRL1 is pull up by external resistor. 1: FANCTRL1is pull down by internal 100KΩ resistor.

S: Register default values are decided by trapping.

6.10.6 Fan1 Base Temperature Register – Index 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description

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7-0	FAN1_BASE _TEMP	R/W	3VA	0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL (CR9F [7]) must set to “1”.

6.10.7 FAN1 Temperature Adjustment Rate Register — Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	Reserved	-	-	-	Reserved
6-4	TFAN1_ADJ_UP _RATE		3VA	3’h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.
3	Reserved	-		-	Reserved
2-0	TFAN1_ADJ_DN _RATE	R/W	3VA	3’h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3’h1: 1 (Ct = 1) 3’h2: 1/2 (Ct= 1/2) 3’h3: 1/4 (Ct = 1/4) 3’h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to “1”.

6.10.8 FAN mode Select Register — Index 96h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	--	-	0	Reserved
5-4	FAN3_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xC6-0xCE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xC6-0xCE. 10: Manual mode fan control. User can write expected **RPM** count to 0xC2-0xC3, and F81768 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control. User can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xC3, and F81768 will output this desired duty or voltage to control fan speed.

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3-2	FAN2_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xB6-0xBE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** (voltage) defined in 0xB6-0xBE. 10: Manual mode fan control. User can write expected **RPM** count to 0xB2-0xB3, and F81768 will adjust duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F81768 will output this desired duty or voltage to control fan speed.
1-0	FAN1_MODE	R/W	VBAT	01	00: Auto fan speed control. Fan speed will follow different temperature by different **RPM** defined in 0xA6-0xAE. 01: Auto fan speed control. Fan speed will follow different temperature by different **duty cycle** defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F81768 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed automatically. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F81768 will output this desired duty or voltage to control fan speed.

6.10.9 FAN mode Select Register — Index 96h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	-		-	Reserved
5	FREQ_SEL_ADD3	R/W	3VA	0	This bit and FAN3_PWM_FREQ_SEL are used to select FAN3 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
4	FREQ_SEL_ADD2	R/W	3VA	0	This bit and FAN2_PWM_FREQ_SEL are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
3	FREQ_SEL_ADD1	R/W	3VA	0	This bit and FAN1_PWM_FREQ_SEL are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz

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2-0	TFAN1_ADJ_SEL	R/W	3VA	0h	This selects which temperature to be used as Ta for Fan1 temperature adjustment. 000: PECI (CR7Eh) 001: T1 (CR72h) 010: T2 (CR74h) 011: T3 (CR76h) 100: TSI CPU temperature (CR7Ah) 101:MXM temperature (CR7Bh). 110: Reserved. 111: Reserved. otherwise: Ta will be 0. To access this register FAN_PROG_SEL must set to “1”.

6.10.10 Auto FAN1 and FAN2 Boundary Hystersis Select Register — Index 98h

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_HYS	R/W	3VA	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	3VA	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

6.10.11 Auto FAN3 Boundary Hystersis Select Register — Index 99h

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	--	-	0	Reserved
3-0	FAN3_HYS	R/W	3VA	4h	Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

6.10.12 Auto Fan Up Speed Update Rate Select Register — Index 9Ah

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	--	-	0	Reserved
5-4	FAN3_UP_RATE	R/W	3VA	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_UP_RATE	R/W	3VA	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

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1-0	FAN1_UP_RATE	R/W	3VA	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

6.10.13 Auto Fan Down Speed update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 0)

Bit	Name	R/W	Reset	Default	Description
7-6	Reserved	--	-	0	Reserved
5-4	FAN3_DN_RATE	R/W	3VA	01	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DN_RATE	R/W	3VA	01	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DN_RATE	R/W	3VA	01	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

6.10.14 Auto Fan Down Speed update Rate Select Register — Index 9Bh (FAN_PROG_SEL = 1)

Bit	Name	R/W	Reset	Default	Description
7	UP_DN_RATE_EN	R/W	3VA	0	0: Fan down rate disable 1: Fan down rate enable Set this bit 1 to use different fan up/down rate. If this bit is not set to 1, the fan up/down rate will follow FAN_UP_RATE.
6	DIRECT_LOAD_EN	R/W	3VA	0	0: Direct load disable 1: Direct load enable for manual duty mode
5-0	Reserved	-	-	-	Reserved

6.10.15 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Reset	Default	Description
7-4	FAN2_STOP _DUTY	R/W	3VA	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

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3-0	FAN1_STOP _DUTY	R/W	3VA	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

6.10.16 FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Reset	Default	Description
7-4	Reserved	--	-	0	Reserved
3-0	FAN3_STOP_ DUTY	R/W	3VA	5h	When fan start, the FAN_CTRL3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

6.10.17 FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Index 9Eh

Bit	Name	R/W	Reset	Default	Description
7-0	PROG_DUTY_VAL	R/W	VBAT	66h/ FFh	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down. Default value is powered on strapped by FAN_40_100.

6.10.18 Fan Fault Time Register — Index 9Fh

Bit	Name	R/W	Reset	Default	Description
7	FAN_PROG_SEL	R/W	3VA	0	Set this bit to “1” will enable accessing registers of other bank.
6	FAN_MNT_SEL	R/W	3VA	0	Set this bit to monitor a slower fan.
5	Reserved	-	-	-	Reserved
4	FAN40_100_SEL	RO	3VCC	-	This bit is the power on trap value of FAN40_100.
3-0	F_FAULT_TIME	R/W	3VA	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can’t reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0, means 1 seconds; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

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6.11 Fan1 Detail Setting

6.11.1 FAN1 Index A0h~AFh

Address	Attribute	Reset	Default	Description
A0h	RO	3VCC	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	3VCC	8'hff	FAN1 count reading (LSB).
A2h	R/W	3VA	8'h00	RPM mode(CR96 bit0=0): FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. Duty mode(CR96 bit0=1): This byte is reserved byte.
A3h	R/W	3VA	8'h01	RPM mode(CR96 bit0=0): FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit0=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	3VA	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	3VA	8'hff	FAN1 full speed count reading (LSB).

6.11.2 VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP1	R/W	3VA	3Ch (60°C)	The first boundary temperature for VT1 in temperature mode. When VT1 temperature **exceeds** this boundary, expected FAN1 value will be loaded from segment **1** register (index AAh). When VT1 temperature is **under** this boundary – hysteresis, expected FAN1 value will be loaded from segment **2** register (index ABh). This byte is a 2's complement value ranged from -128°C ~ 127°C.

6.11.3 VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP1	R/W	3VA	32 (50°C)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 2 register (index ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 3 register (index ACh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

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6.11.4 VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP1	R/W	3VA	28h (40°C)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 3 register (index ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 4 register (index ADh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.11.5 VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP1	R/W	3VA	1Eh (30°C)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 4 register (index ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.11.6 FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED1	R/W	3VA	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.11.7 FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED1	R/W	3VA	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.11.8 FAN1 SEGMENT 3 SPEED COUNT Register – Index ACh

Bit	Name	R/W	Reset	Default	Description

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7-0	SEC3SPEED1	R/W	3VA	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.11.9 FAN1 SEGMENT 4 SPEED COUNT Register – Index ADh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED1	R/W	3VA	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.11.10 FAN1 SEGMENT 5 SPEED COUNT Register – Index AEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED1	R/W	3VA	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.11.11 FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Reset	Default	Description
7	FAN1_TEMP _SEL_DIG	R/W	3VA	0	This bit companies with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	FAN1_PWM _FREQ_SEL	R/W	3VA	0	This bit and FREQ_SEL_ADD1 are used to select FAN1 PWM frequency. NEW_FREQ_SEL1 = { FREQ_SEL_ADD1, FAN1_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN1_UP_T_EN	R/W	3VA	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_ INTERPOLATION_E N	R/W	3VA	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP _HIGH_EN	R/W	3VA	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.

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2	FAN1_JUMP _LOW_EN	R/W	3VA	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	3VA	01	This registers company with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 100: fan1 follows TSI CPU temperature (CR7Ah) 101: fan1 follows MXM temperature (CR7Bh). Others are reserved.

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6.12 Fan2 Detail Setting

6.12.1 FAN2 Index B0h~BFh

Address	Attribute	Reset	Default Value	Description
B0h	RO	3VCC	8'h0F	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	3VCC	8'hFF	FAN2 count reading (LSB).
B2h	R/W	3VA	8'h00	RPM mode(CR96 bit2=0): FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. Duty mode (CR96 bit2=1): This byte is reserved byte.
B3h	R/W	3VA	8'h01	RPM mode(CR96 bit2=0): FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit2=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	3VA	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	3VA	8'hFF	FAN2 full speed count reading (LSB).

6.12.2 VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP2	R/W	3VA	3Ch (60°C)	The first boundary temperature for VT2 in temperature mode. When VT2 temperature **exceeds** this boundary, FAN2 expect value will load from segment **1** register (index Bah). When VT2 temperature is **under** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BAh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.12.3 VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP2	R/W	3VA	32 (50°C)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 2 register (index BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

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6.12.4 VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP2	R/W	3VA	28h (40°C)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 3 register (index BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.12.5 VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP2	R/W	3VA	1Eh (30°C)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 4 register (index BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C.

6.12.6 FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED2	R/W	3VA	FFh (100%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.7 FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED2	R/W	3VA	D9h (85%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.8 FAN2 SEGMENT 3 SPEED COUNT Register – Index BCh

Bit	Name	R/W	Reset	Default	Description

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7-0	SEC3SPEED2	R/W	3VA	B2h (70%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.9 FAN2 SEGMENT 4 SPEED COUNT Register – Index BDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED2	R/W	3VA	99h (60%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.10 FAN2 SEGMENT 5 SPEED COUNT Register – Index BEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5PEED2	R/W	3VA	80h (50%)	The meaning of this register is depending on the FAN2_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.12.11 FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Reset	Default	Description
7	FAN2_TEMP_ SEL_DIG	R/W	3VA	0	This bit companies with FAN2_TEMP_SEL to select the temperature source for controlling FAN2.
6	FAN2_PWM_ FREQ_SEL	R/W	3VA	0	This bit and FREQ_SEL_ADD2 are used to select FAN2 PWM frequency. NEW_FREQ_SEL2 = { FREQ_SEL_ADD2, FAN2_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN2_UP_T_EN	R/W	3VA	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_ INTERPOLATION_EN	R/W	3VA	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_ HIGH_EN	R/W	3VA	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.

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2	FAN2_JUMP_LOW_EN	R/W	3VA	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.
1-0	FAN2_TEMP_SEL	R/W	3VA	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 3 (CR76h). 100: fan2 follows TSI CPU temperature (CR7Ah) 101: fan2 follows MXM temperature (CR7Bh). Otherwise: reserved.

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6.13 Fan 3 Detail Setting

6.13.1 FAN3 Index C0h- CFh

Address	Attribute	Reset	Default Value	Description
C0h	RO	3VCC	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	3VCC	8'hFF	FAN3 count reading (LSB).
C2h	R/W	3VA	8'h00	RPM mode(CR96 bit4=0): FAN3 expect speed count value (MSB), in auto fan mode (CR96 bit5➔0) this register is auto updated by hardware. Duty mode(CR96 bit4=1): This byte is reserved byte.
C3h	R/W	3VA	8'h01	RPM mode(CR96 bit4=0): FAN3 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. Duty mode(CR96 bit4=1): The Value programming in this byte is duty value. In auto fan mode (CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	3VA	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	3VA	8'hFF	FAN3 full speed count reading (LSB).

6.13.2 VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND1TMP3	R/W	3VA	3Ch (60^{o}C)	The first boundary temperature for VT3 in temperature mode. When VT3 temperature **exceeds** this boundary, FAN3 expect value will load from segment **1** register (index CAh). When VT3 temperature is **under** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (index CAh). This byte is a 2's complement value ranging from -128^{o}C ~ 127^{o}C.

6.13.3 VT3 BOUNDARY 2 TEMPERATURE – Index C7

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND2TMP3	R/W	3VA	32 (50^{o}C)	The 2nd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 2 register (index CBh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 3 register (index CCh). This byte is a 2's complement value ranging from-128^{o}C ~ 127^{o}C.

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6.13.4 VT3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND3TMP3	R/W	3VA	28h (40°C)	The 3rd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 3 register (index CCh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 4 register (index CDh). This byte is a 2's complement value ranging from-128°C ~ 127°C.

6.13.5 VT3 BOUNDARY 4 TEMPERATURE – Index C9h

Bit	Name	R/W	Reset	Default	Description
7-0	BOUND4TMP3	R/W	3VA	1Eh (30°C)	The 4th BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 4 register (index CDh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 5 register (index CEh). This byte is a 2's complement value ranging from-128°C ~ 127°C.

6.13.6 FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC1SPEED3	R/W	3VA	FFh (100%)	The meaning of this register is depending on the FAN3_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex:100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.13.7 FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC2SPEED3	R/W	3VA	D9h (85%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.13.8 FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Reset	Default	Description

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7-0	SEC3SPEED3	R/W	3VA	B2h (70%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.13.9 FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC4SPEED3	R/W	3VA	99h (60%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.13.10 FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Reset	Default	Description
7-0	SEC5SPEED3	R/W	3VA	80h (50%)	The meaning of this register is depending on the FAN3_MODE (CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

6.13.11 FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Reset	Default	Description
7	FAN3_TEMP_ SEL_DIG	R/W	3VA	0	This bit companies with FAN3_TEMP_SEL select the temperature source for controlling FAN3.
6	FAN3_PWM_ FREQ_SEL	R/W	3VA	0	This bit and FREQ_SEL_ADD3 are used to select FAN3 PWM frequency. NEW_FREQ_SEL3 = { FREQ_SEL_ADD3, FAN3_PWM_FREQ_SEL} 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5	FAN3_UP_T_EN	R/W	3VA	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_ INTERPOLATION_EN	R/W	3VA	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_ HIGH_EN	R/W	3VA	1	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.

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2	FAN3_JUMP_LOW_EN	R/W	3VA	1	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	3VA	11	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR7Eh) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 3 (CR76h). 100: fan3 follows TSI CPU temperature (CR7Ah) 101: fan3 follows MXM temperature (CR7Bh). Otherwise: reserved.

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7 Electrical Characteristics

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Power supply voltage range		-0.5	+5.5	V
$V_{I/O}$	Input/output voltage range		-0.5	+3.6	V
T_{stg}	Storage temperature range		-55	150	° C
T_{amb}	Operating temperature	Operating in the free air	-40	85	° C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Static Characteristics

Typical with Ta = 0°C to 70°C, $3V_{CC}$ = 3.3V ± 10%, V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
V_{BAT}	Battery Voltage		2.4	3.3	3.6	V
I_{CC}	Operating Current	$3V_{CC}$=3.3V V_{BAT}=3.3V		10		mA
I_{STY}	Idle State Current	$3V_{CC}$=3.3V V_{BAT}=3.3V		5		uA
I_{BAT}	Battery Current	$3V_{CC}$=3.3V V_{BA}T=3.3V		4		uA

$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, output with12 mA sink capability, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4V		+12		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	μA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			μA

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$I/O_{16t,u47k}$-TTL level bi-directional pin with 16 mA source-sink capability, internal pull-up 47k ohms

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4V		+16		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	μA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			μA

I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{t-}	Input Low Threshold Voltage	V_{DD} = 3.3 V			0.8	V
V_{t+}	Input High Threshold Voltage	V_{DD} = 3.3 V	2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4 V		-12	-9	mA
I_{OH}	Output High Current	V_{OH} = 2.4V	+9	+12		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	μA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			μA

$I/OOD_{12t,5v}$-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function, 5v tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{t-}	Input Low Threshold Voltage	V_{DD} = 3.3 V			0.8	V
V_{t+}	Input High Threshold Voltage	V_{DD} = 3.3 V	2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4 V		-12	-9	mA
I_{OH}	Output High Current	V_{OH} = 2.4V	+9	+12		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	μA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			μA

$I/OOD_{8st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 8mA source-sink capability, 5v tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{t-}	Input Low Threshold Voltage	V_{DD} = 3.3 V			0.8	V
V_{t+}	Input High Threshold Voltage	V_{DD} = 3.3 V	2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4 V		-8	-9	mA
I_{OH}	Output High Current	V_{OH} = 2.4V	+9	+8		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	μA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			μA

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I/$OOD_{12st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 12mA source-sink capability, 5v tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{t-}	Input Low Threshold Voltage	V_{DD} = 3.3 V			0.8	V
V_{t+}	Input High Threshold Voltage	V_{DD} = 3.3 V	2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4 V		-12	-9	mA
I_{OH}	Output High Current	V_{OH} = 2.4V	+9	+12		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	µA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			µA

I/$OOD_{24st,5v}$-TTL level bi-directional pin and schmitt triggrt, Open-drain output with 24mA source-sink capability, 5v tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{t-}	Input Low Threshold Voltage	V_{DD} = 3.3 V			0.8	V
V_{t+}	Input High Threshold Voltage	V_{DD} = 3.3 V	2.0			V
I_{OL}	Output Low Current	V_{OL} = 0.4 V		-24	-9	mA
I_{OH}	Output High Current	V_{OH} = 2.4V	+9	+24		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	µA
I_{LIL}	Input Low Leakage	V_{IN} = 0V	-1			µA

IN_{st} - TTL level input pin with schmitt trigger

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	µA
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			µA

$IN_{t,5v}$ - TTL level input pin with 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	µA
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			µA

$IN_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	µA
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			µA

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$IN_{st,u47k}$ - TTL level input pin with schmitt trigger, internal pull-up 47k ohms

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{LIH}	Input High Leakage	$V_{IN} = V_{DD}$			+1	μA
I_{LIL}	Input Low Leakage	$V_{IN} = 0$ V	-1			μA

$IN_{st,u47k}$ - TTL level input pin with schmitt trigger, internal pull-up 47k ohms

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{LIH}	Input High Leakage	$V_{IN} = V_{DD}$			+1	μA
I_{LIL}	Input Low Leakage	$V_{IN} = 0$ V	-1			μA

OD_{12}-Open-drain output with12 mA sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	$V_{OL} = 0.4$V		-12		mA

OD_{12}-Open-drain output with12 mA sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	$V_{OL} = 0.4$V		-12		mA

OD_{14}-Open-drain output with14 mA sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	$V_{OL} = 0.4$V		-14		mA

OD_{24}-Open-drain output with24 mA sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	$V_{OL} = 0.4$V		-24		mA

$OD_{12,u10k,5v}$-Open-drain output with 12 mA sink capability, pull-up 10k ohms, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	$V_{OL} = 0.4$V		-12		mA

$OD_{12,u10k,5v}$-Open-drain output with 12 mA sink capability, pull-up 10k ohms, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	$V_{OL} = 0.4$V		-12		mA

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$OD_{16,u10k,5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OL}	Output Low Current	V_{OL} = 0.4V		-16		mA

$O_{8t,u47,5v}$- TTL level Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V	+6	+8		mA

O_{12}- Output pin with 12 mA source-sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V	+9	+12		mA

O_{16}- Output pin with 16 mA source-sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V		+16		mA

O_{18}- Output pin with 18 mA source-sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V		+18		mA

O_{20}- Output pin with 20 mA source-sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V		+20		mA

O_{30}- Output pin with 30 mA source-sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V	+26	+30		mA

$O_{12,5v}$- Output pin with 12 mA source-sink capability, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
I_{OH}	Output High Current	V_{OL} = 0.4V	+9	+12		mA

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$I_{LV}/O_{D8,s1}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.). Output with 8mA drive and 1mA sink capability

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		0.9			V
I_{OH}	Output High Current	V_{OH} = 1.0V		+8		mA
I_{LIH}	Input High Leakage	$V_{IN} = V_{DD}$			+1	A
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			A

$I/OD_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{OH}	Output High Current	V_{OH} = 1.0V		+12		mA
I_{LIH}	Input High Leakage	$V_{IN} = V_{DD}$			+1	A
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			A

$I/OD_{14st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{OH}	Output High Current	V_{OH} = 0.4V		+14		mA
I_{LIH}	Input High Leakage	$V_{IN} = V_{DD}$			+1	A
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			A

$I/OD_{16st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{OH}	Output High Current	V_{OH} = 0.4V		+16		mA
I_{LIH}	Input High Leakage	$V_{IN} = V_{DD}$			+1	A
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			A

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I_{Lv} /$OD_{12st,5v}$-Low level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance

Symbol	Parameter	Conditions	Min	Typ	Max	UNIT
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		0.9			V
I_{OH}	Output High Current	V_{OH} = 0.4V		+12		mA
I_{LIH}	Input High Leakage	V_{IN} = V_{DD}			+1	A
I_{LIL}	Input Low Leakage	V_{IN} = 0 V	-1			A

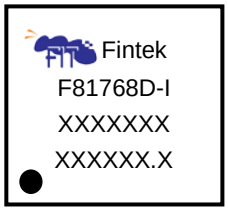
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8 Ordering Information

Part Number	Package Type
F81768D-I	128-LQFP (Green Package)

9 Top Marking Specification

The version identification is shown as the bold red three characters. Please refer to below table for detail:



Fintek Logo

● Pin 1 Location

1st Line: Device Name → **F81768D-I. "D" means LQFP package, "-I" means industrial specification.**

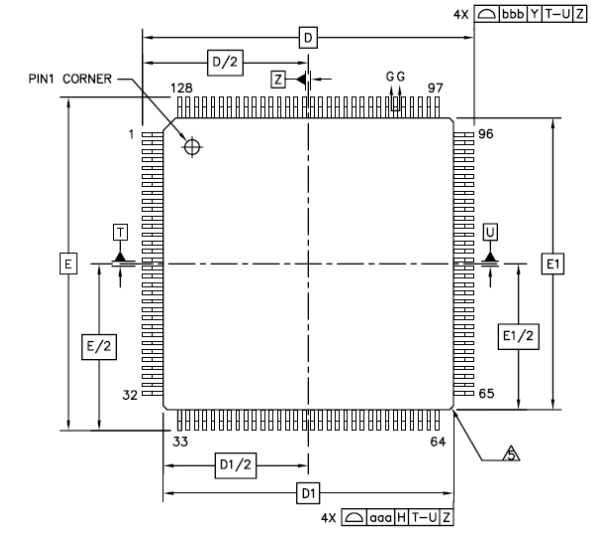
2nd Line: Assembly Plant Code (x) + Assembled Year Code (x) + Week Code (xx) + Fintek Internal Code (xx) + IC Version (x) where A means version A, B means version B,

3rd Line: Wafer Fab Code (XXXX…XX)

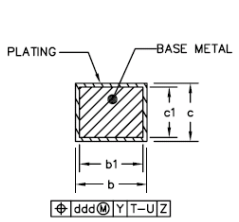
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10 Package Dimension

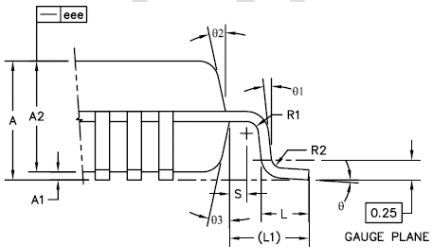
128-LQFP



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



SECTION G-G
SCALE: 100/1



DETAIL F
SCALE: 20/1

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

Feature Integration Technology Inc.

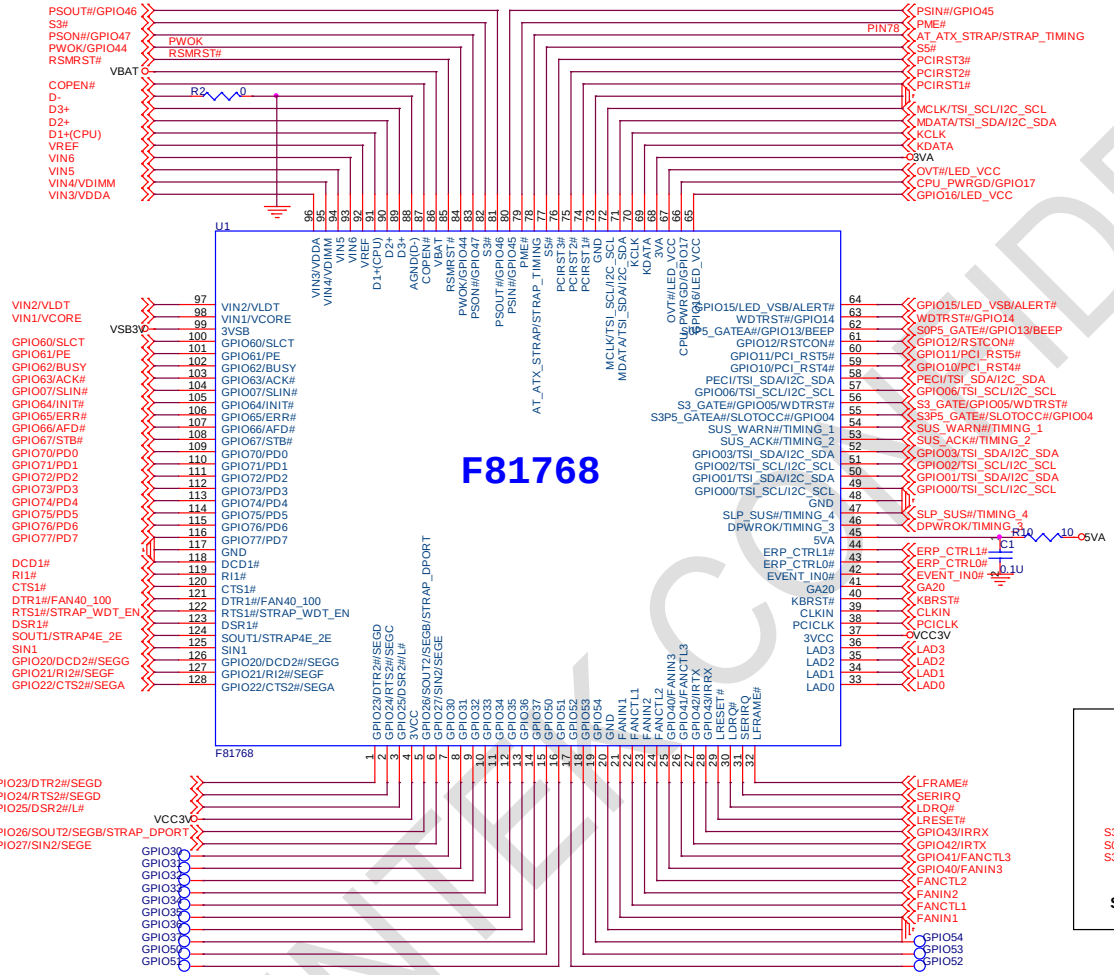
Headquarters
3F-7, No 36, Tai Yuan St.,
Chupei City, Hsinchu, Taiwan 302, R.O.C.
TEL : 886-3-5600168
FAX : 886-3-5600166
www: http://www.fintek.com.tw

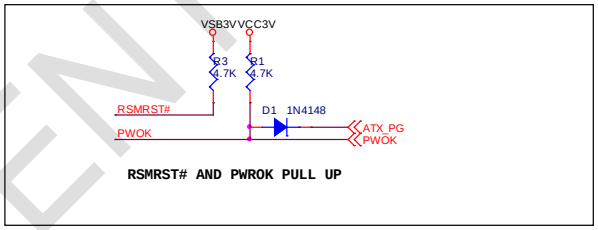
Taipei Office
Bldg. K4, 7F, No.700, Chung Cheng Rd.,
Chungho City, Taipei, Taiwan 235, R.O.C.
TEL : 866-2-8227-8027
FAX : 866-2-8227-8037

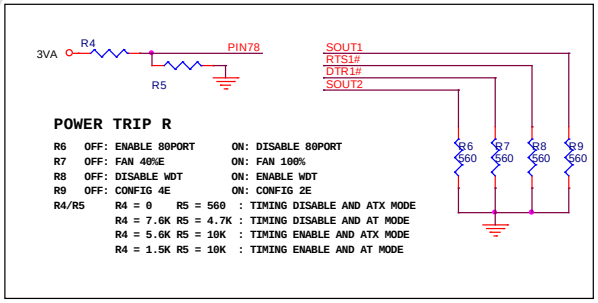
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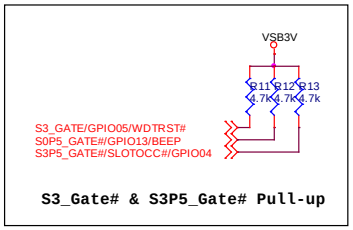
11 Demo Circuit

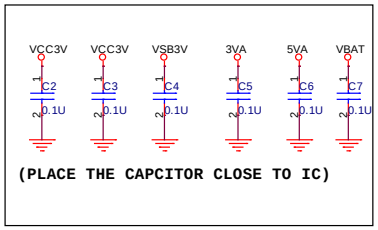
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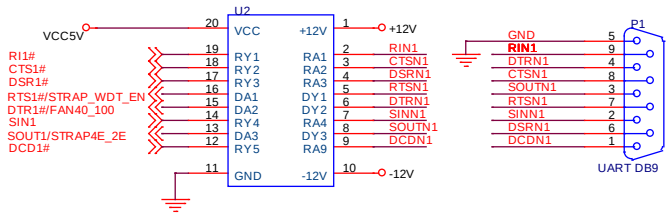




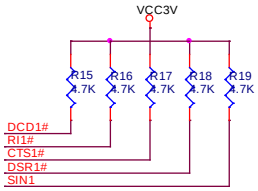


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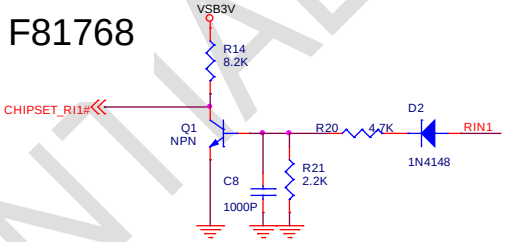


UART 1 PORT INTERFACE

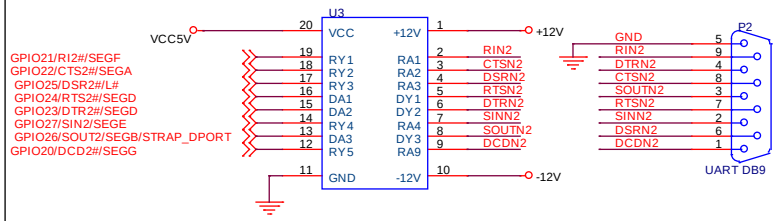


If you do not use the UART port 1, please pull-up these pin to VCC3V.

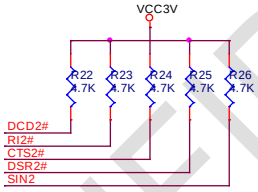
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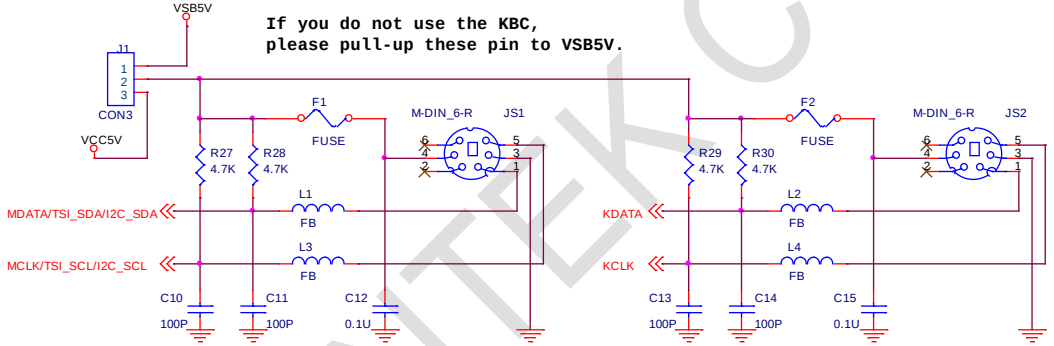
Wake up on ring for serial port circuit.



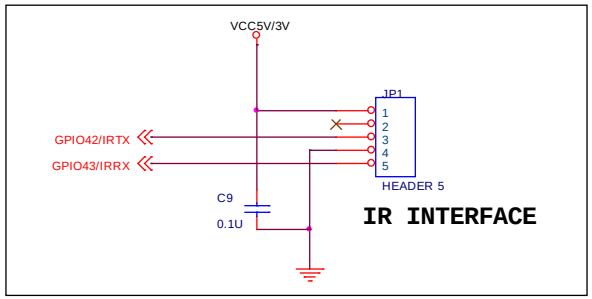
UART 2 PORT INTERFACE



If you do not use the UART port 2, please pull-up these pin to VCC3V.



PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

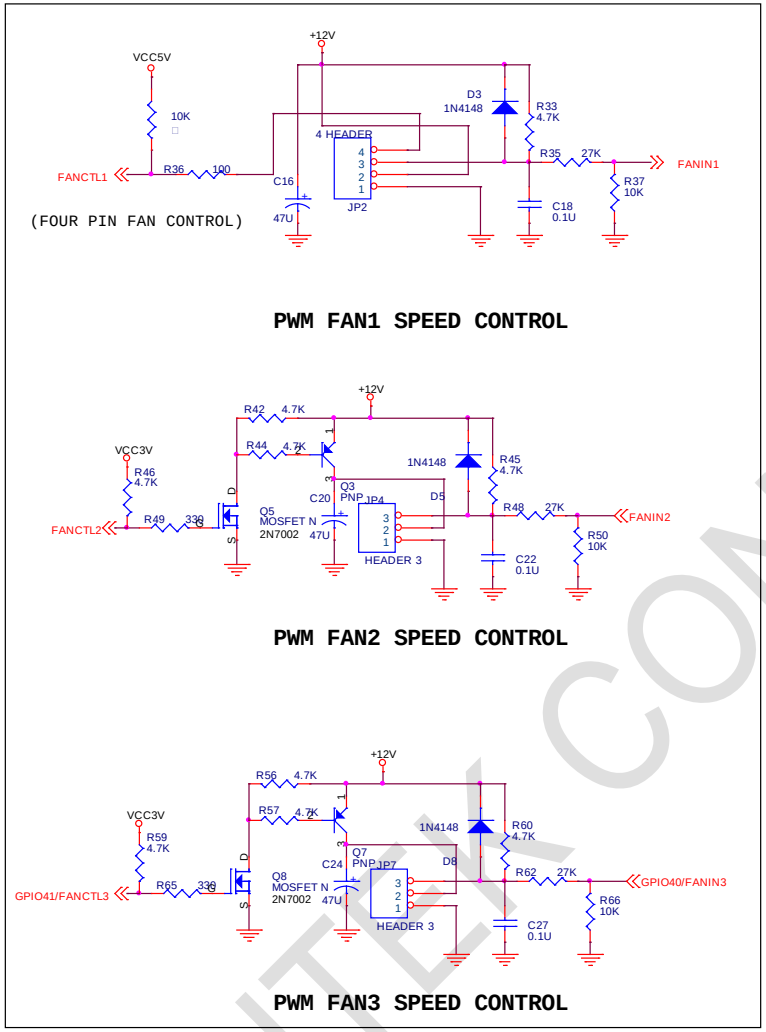


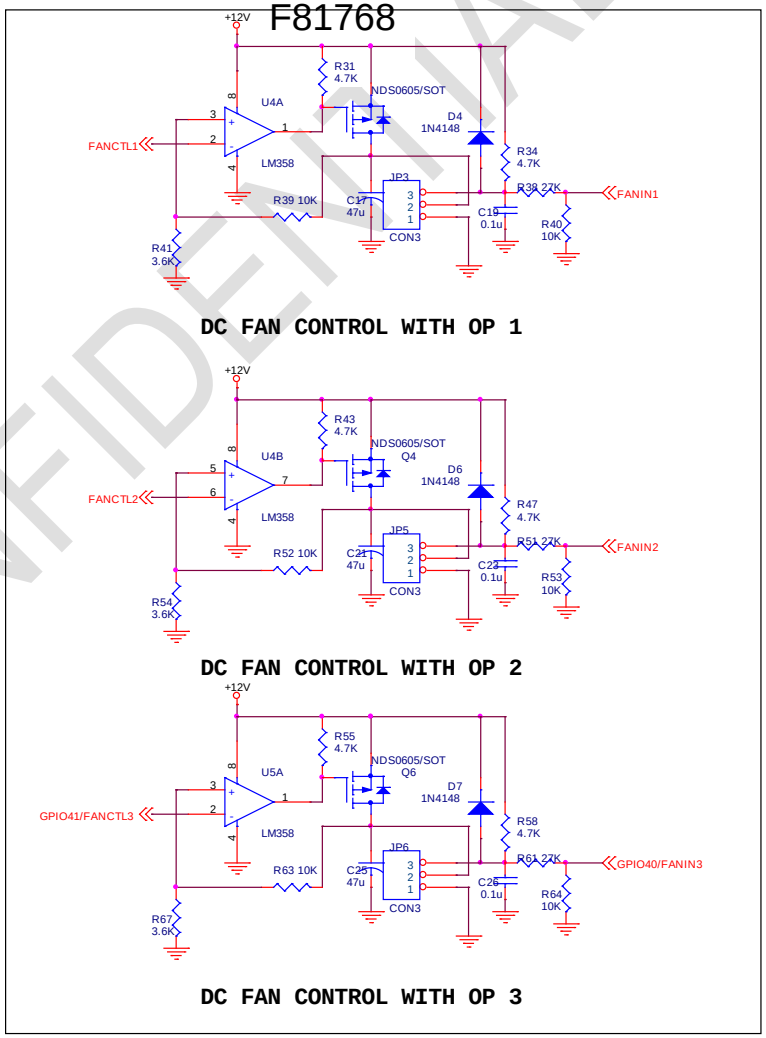
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Date: Thursday, February 21, 2013	Sheet 2 of 7	

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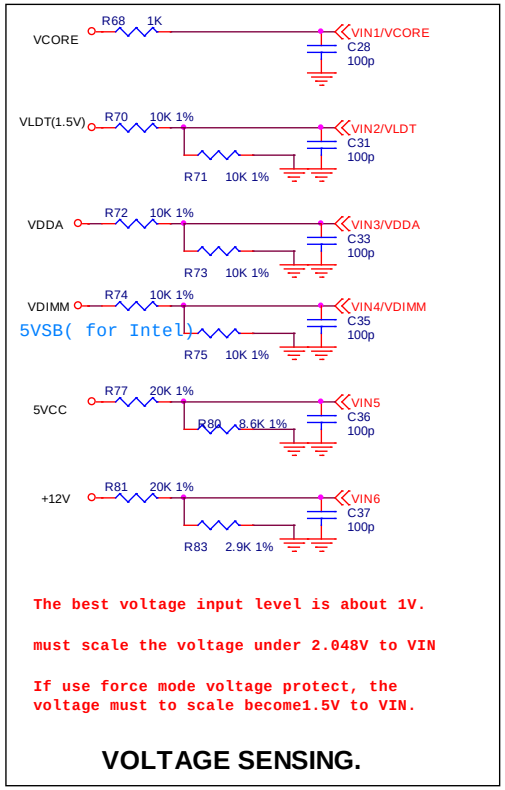


FAN CONTROL FOR PWM OR DC

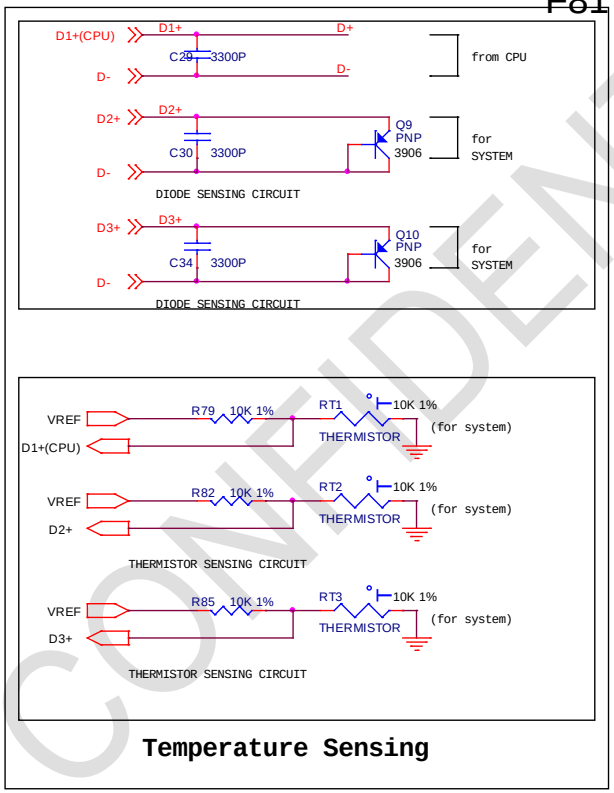
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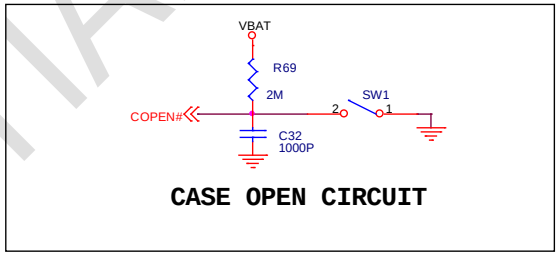
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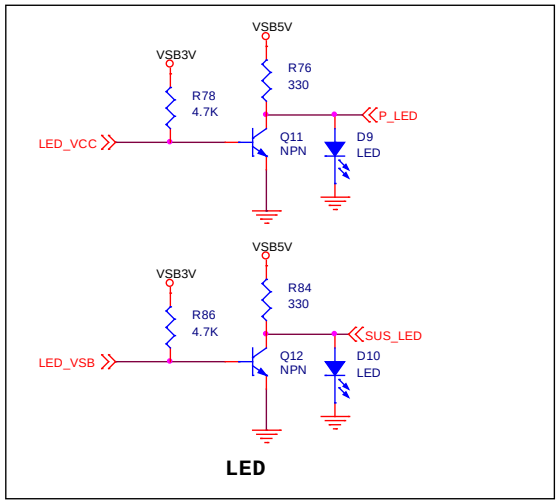
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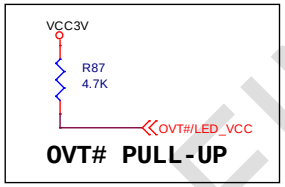
Temperature Sensing



CASE OPEN CIRCUIT



LED

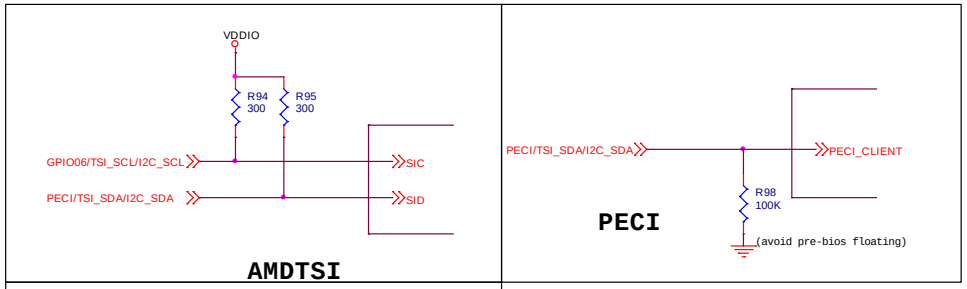


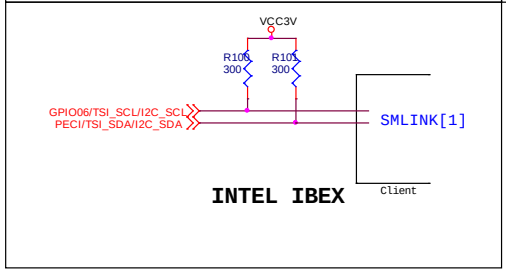
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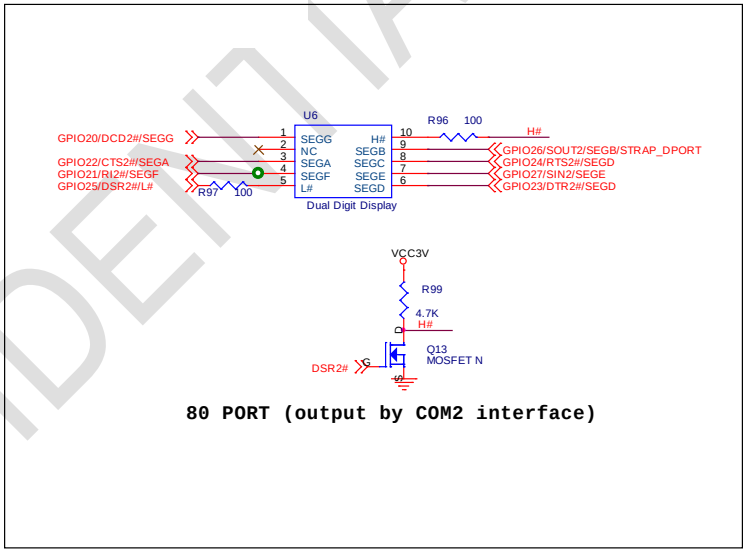
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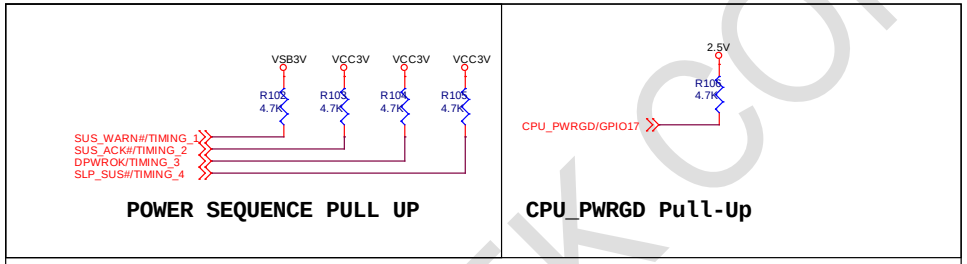
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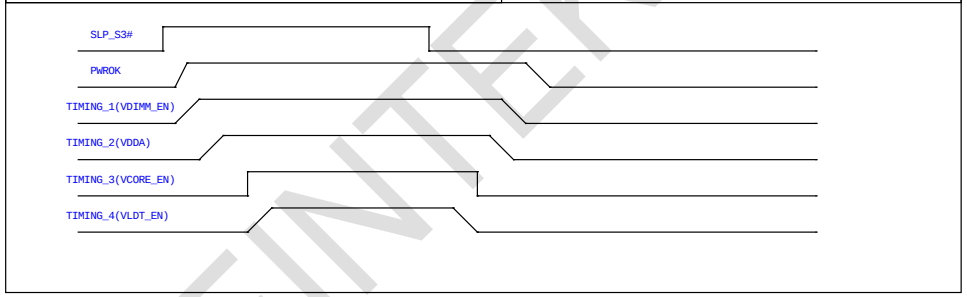
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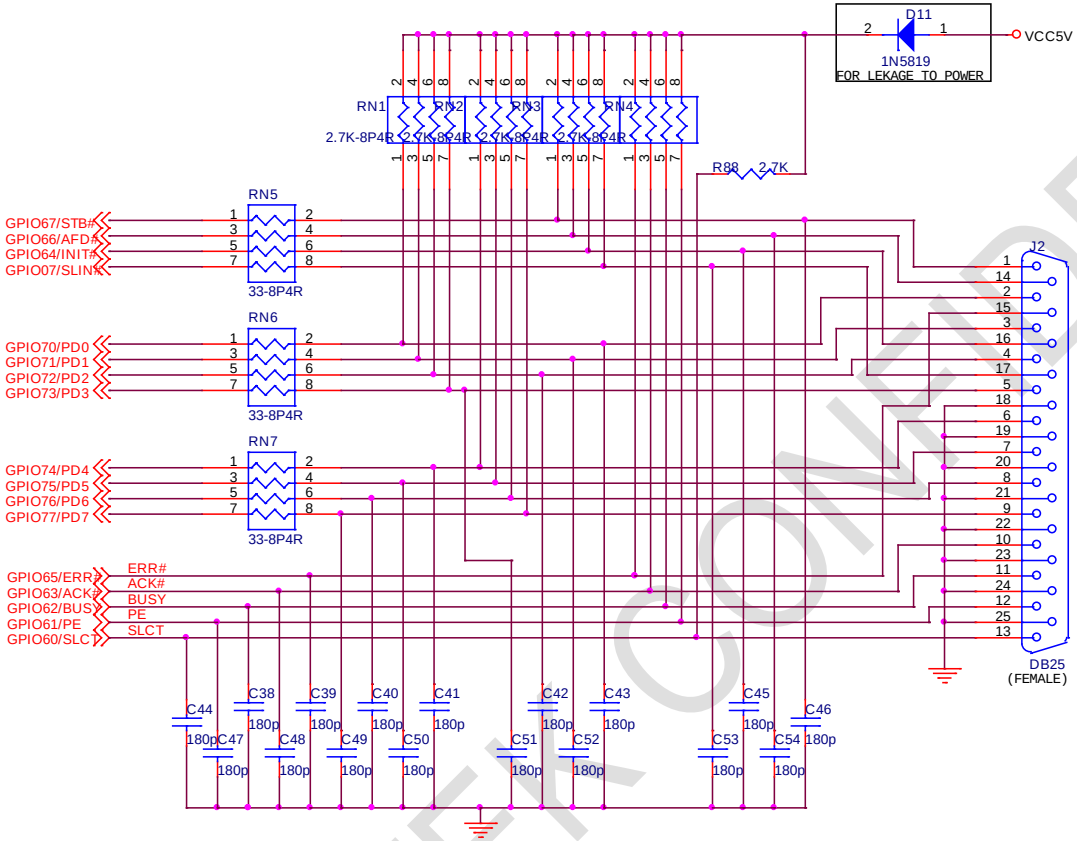




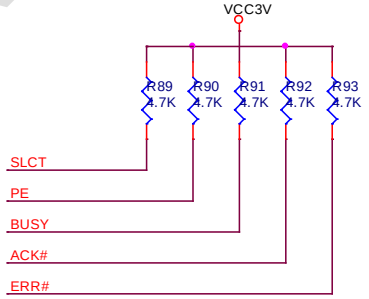
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PARALLEL PORT INTERFACE

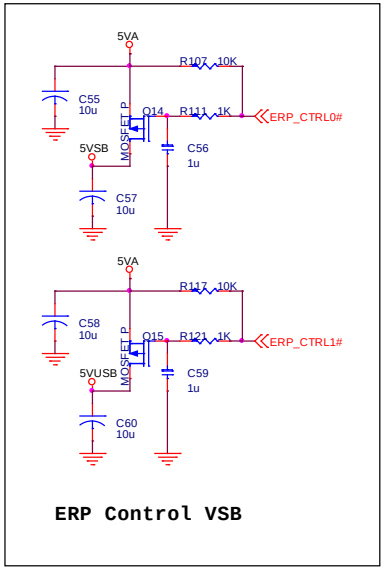


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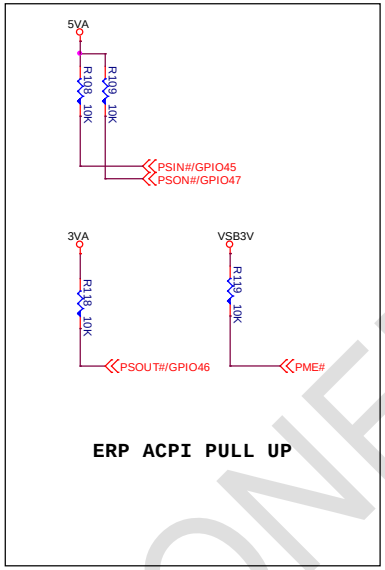
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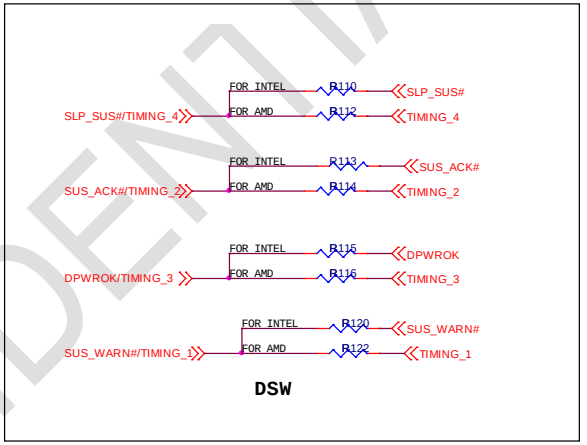
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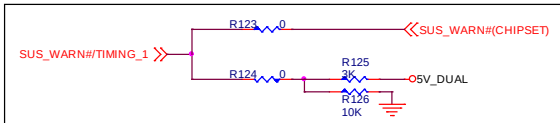
ERP Control VSB



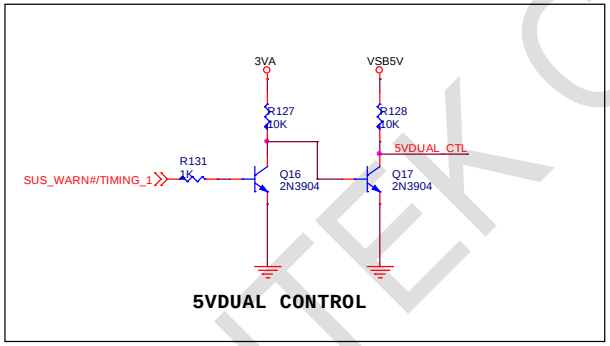
ERP ACPI PULL UP



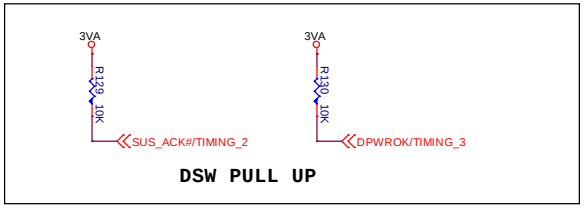
DSW



Select SUS_WARN# to Chipset or 5V_DUAL



5VDUAL CONTROL



DSW PULL UP

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Size: B	Document Number: FINTEK	Rev: <Rev Code>
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